Compal Confidential

QML70 Schematics Document

AMD Comal

APU Trinity / Hudson M3 / Thames XT M2
UMA Only / PX Muxless with BACO

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2011-10-17

LA-8371P REV: 0.2

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Issued Date	2011/07/29	Deciphered Date 2012/07/29	Title: Cover Page
			Size: B; Document Number: QML70 LA-8371P; Rev: 0.2
			Date: Wednesday, October 19, 2011; Sheet 1 of 53

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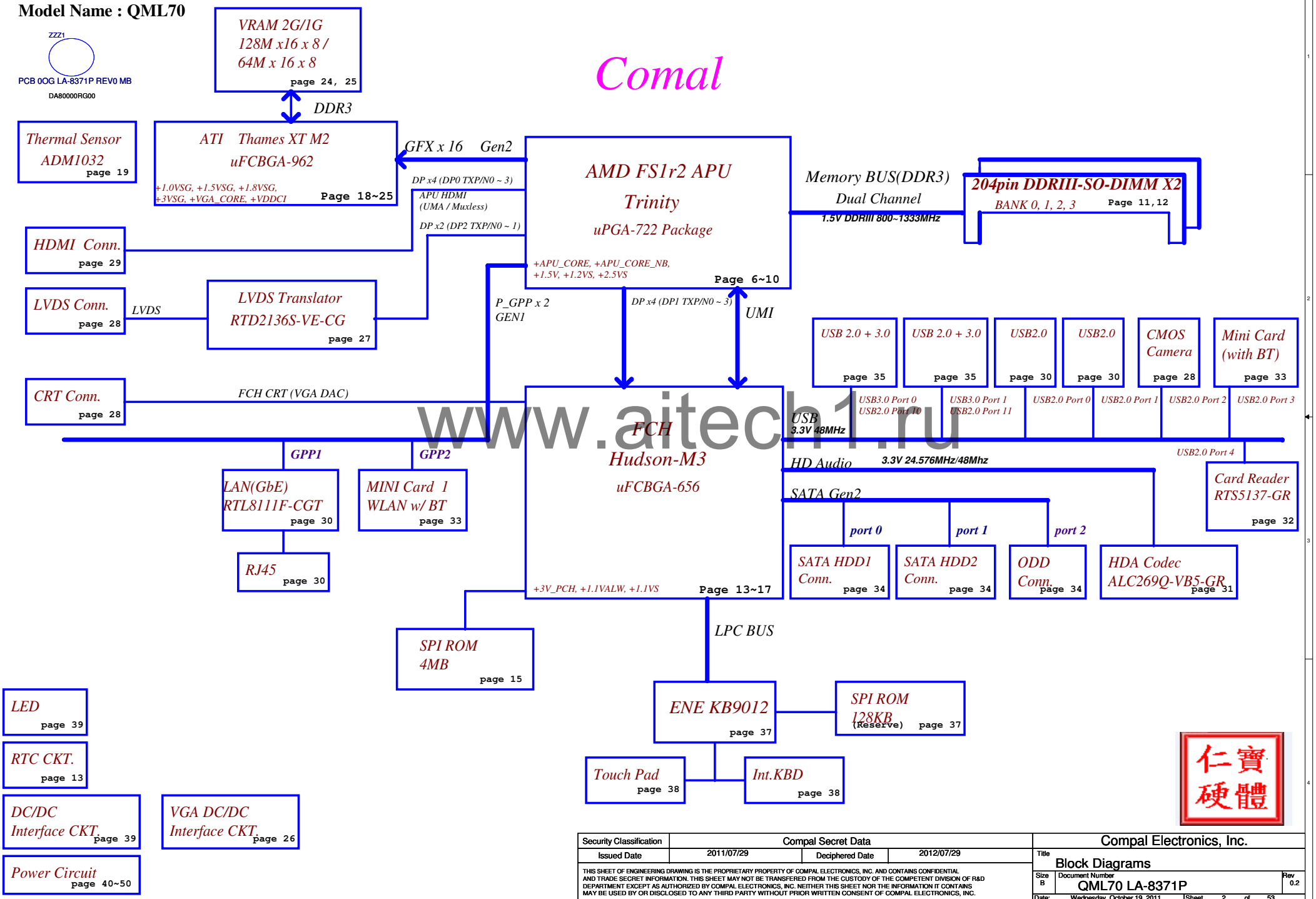
Model Name : QML70



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Title: Block Diagrams

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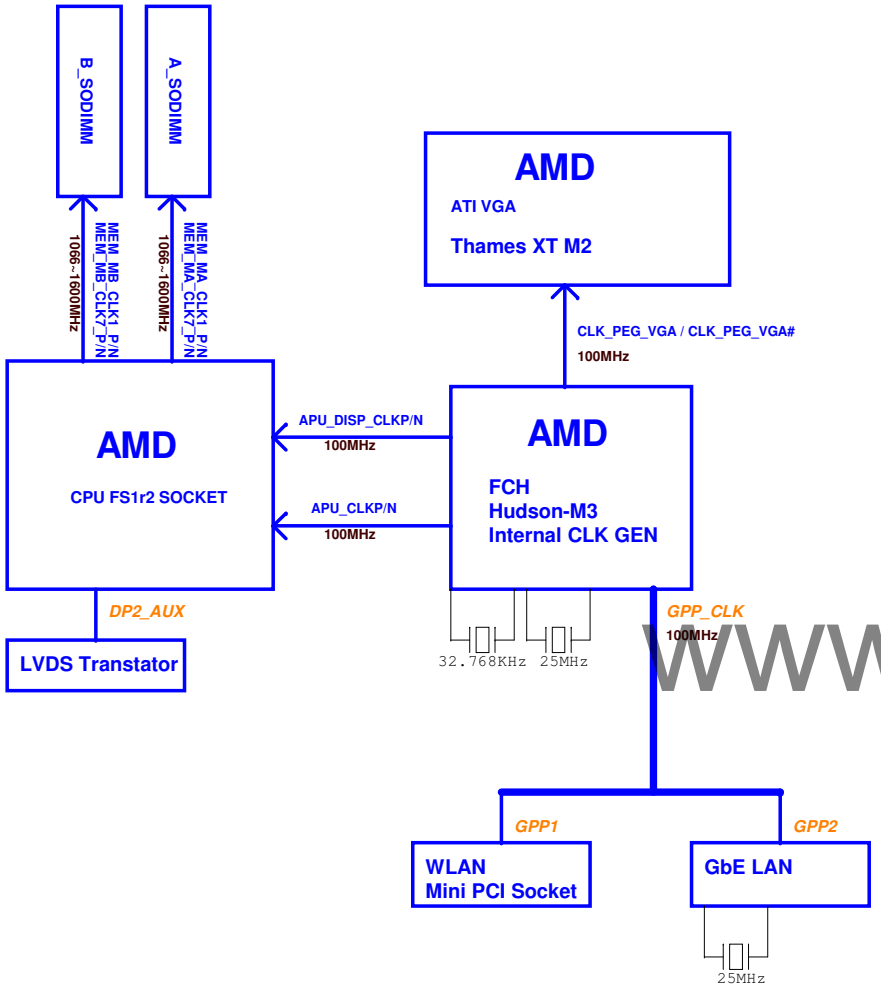
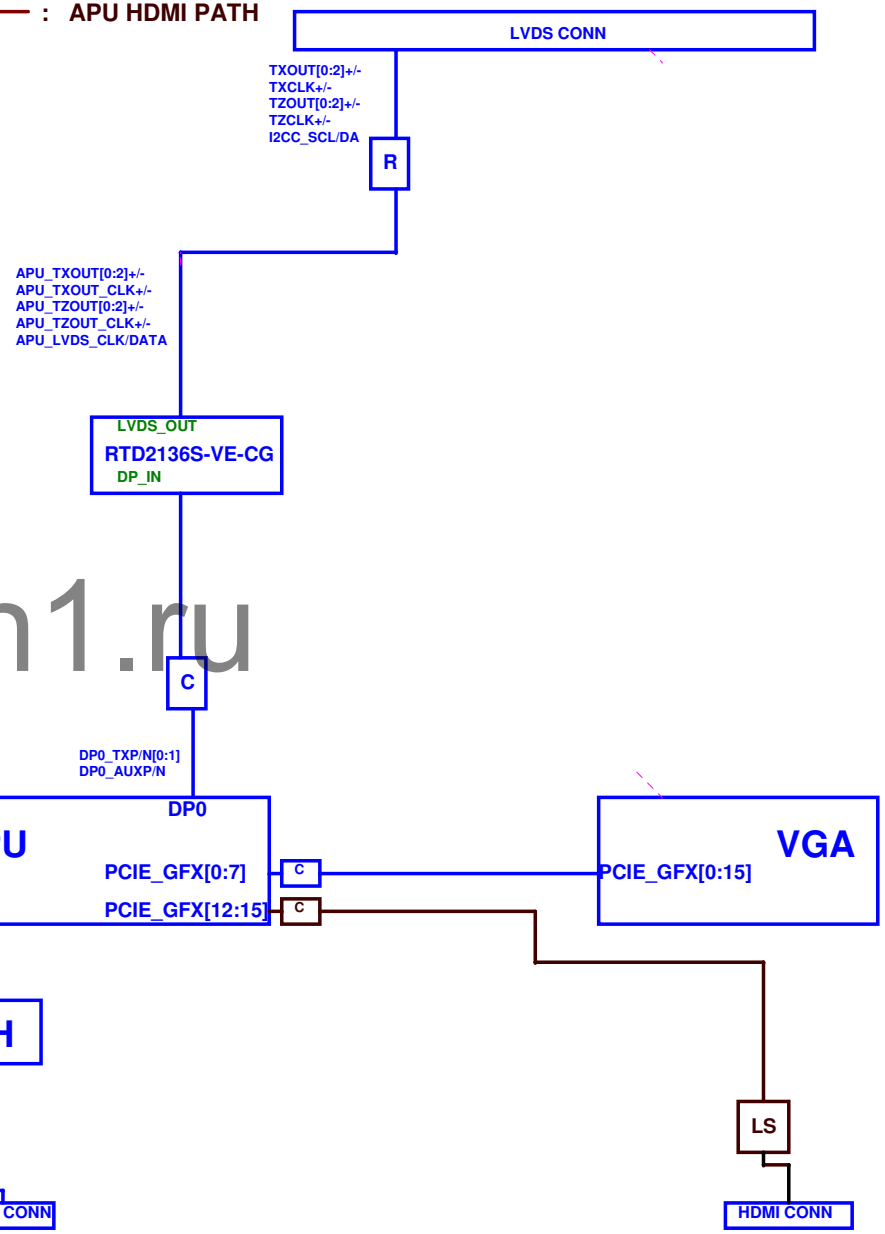
CLOCK DISTRIBUTION



DISPLAY DISTRIBUTION

: LVDS PATH

: APU HDMI PATH



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Title	CLOCK / DISPLAY DISTRIBUTION		
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Voltage Rails

Power Plane	Description	S1	S3	S4/S5	Deep S3
VIN	Adapter power supply (19V)	N/A	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF	ON
+1.0VSG	1.0V switched power rail for VGA	ON	OFF	OFF	OFF
+1.1VALW	1.1V switched power rail for FCH	ON	ON	ON*	OFF
+3V_PCH	3.3V switched power rail for FCH	ON	ON	ON*	OFF
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF	OFF
+3VSG	1.8V switched power rail	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF	ON
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.8VSG	1.8V switched power rail	ON	OFF	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*	ON
+LAN_IO	3.3V power rail for LAN	ON	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*	ON
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*	ON
+RTCVCC	RTC power	ON	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

BOM Structure	BTO Item
PX@	Use VGA (Mux)
X76@	VRAM ID Table
AI	Use AI Charger
nonAI@	Do not use AI Charger
CARD@	Use Card Reader IC
nonCARD@	do not use Card Reader IC
X76L01@	Use Hynix GDDR3 1GB VRAM
X76L02@	Use Hynix GDDR3 2GB VRAM
X76L03@	Use Samsung GDDR3 1GB VRAM
X76L04@	Use Samsung GDDR3 2GB VRAM
930@	Use EC KB930
9012@	Use EC KB9012

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x = 1 is read cmd, x= 0 is writee cmd.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
ADI ADM1032	1001 101X b	9AH
AMD Thames XT M2	1000 001X b	82H
AMD FS1r2 (APU)	1001 1000 b	98H
RTD2132S (TL)	1010 1000 b	A8H

FCH SM Bus 0 address

Device	Address	HEX
DDR DIMM1	1101 000X b	D0
DDR DIMM2	1101 001X b	D2

FCH SM Bus 1 address

Device	Address	HEX

Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra / Rc	100K +/- 5%			
Board ID	Rb / Rd	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0 +/- 5%	0 V	0 V	0.155 V
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V

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Title: Notes List

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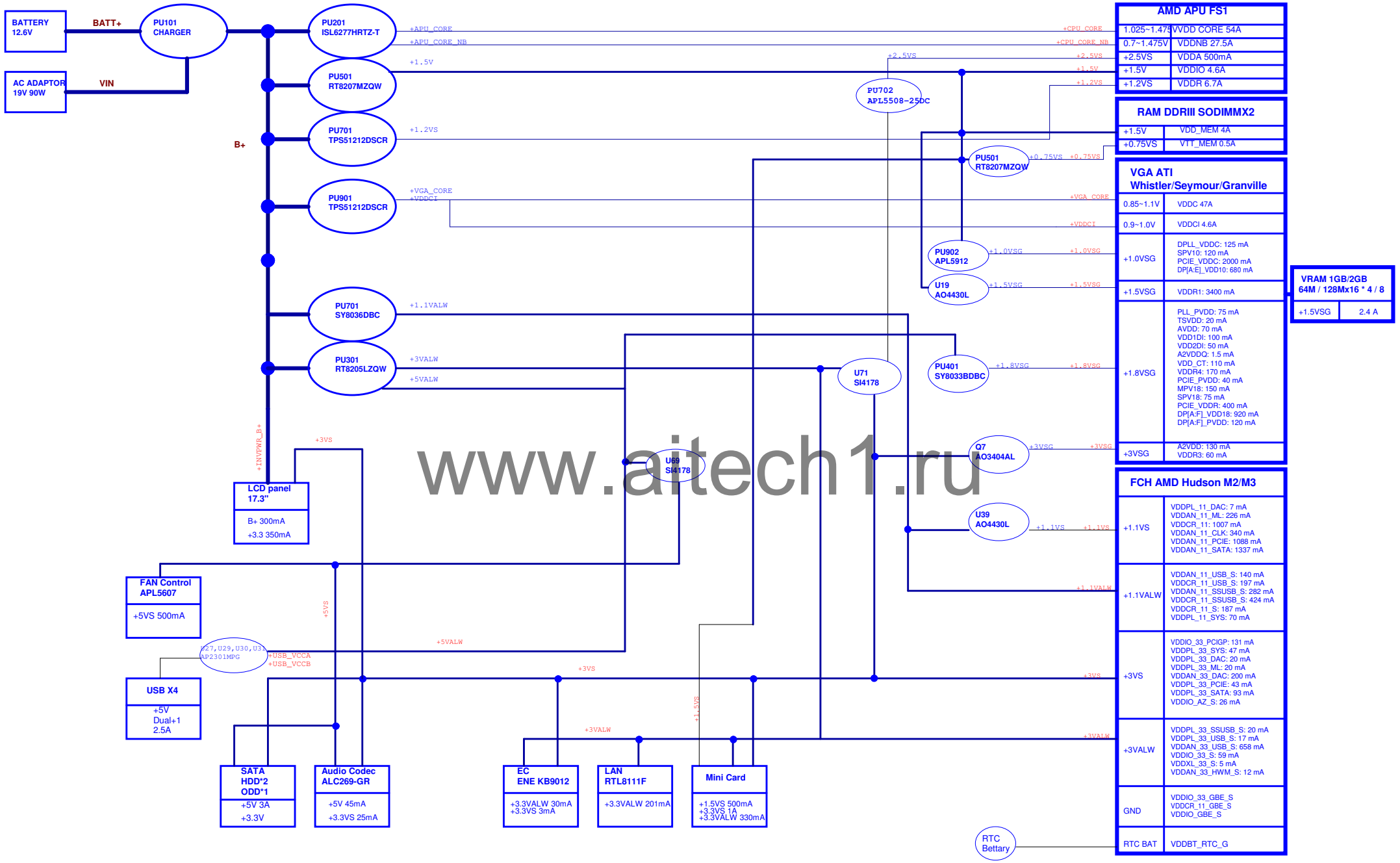

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Title: POWER DELIVERY CHART

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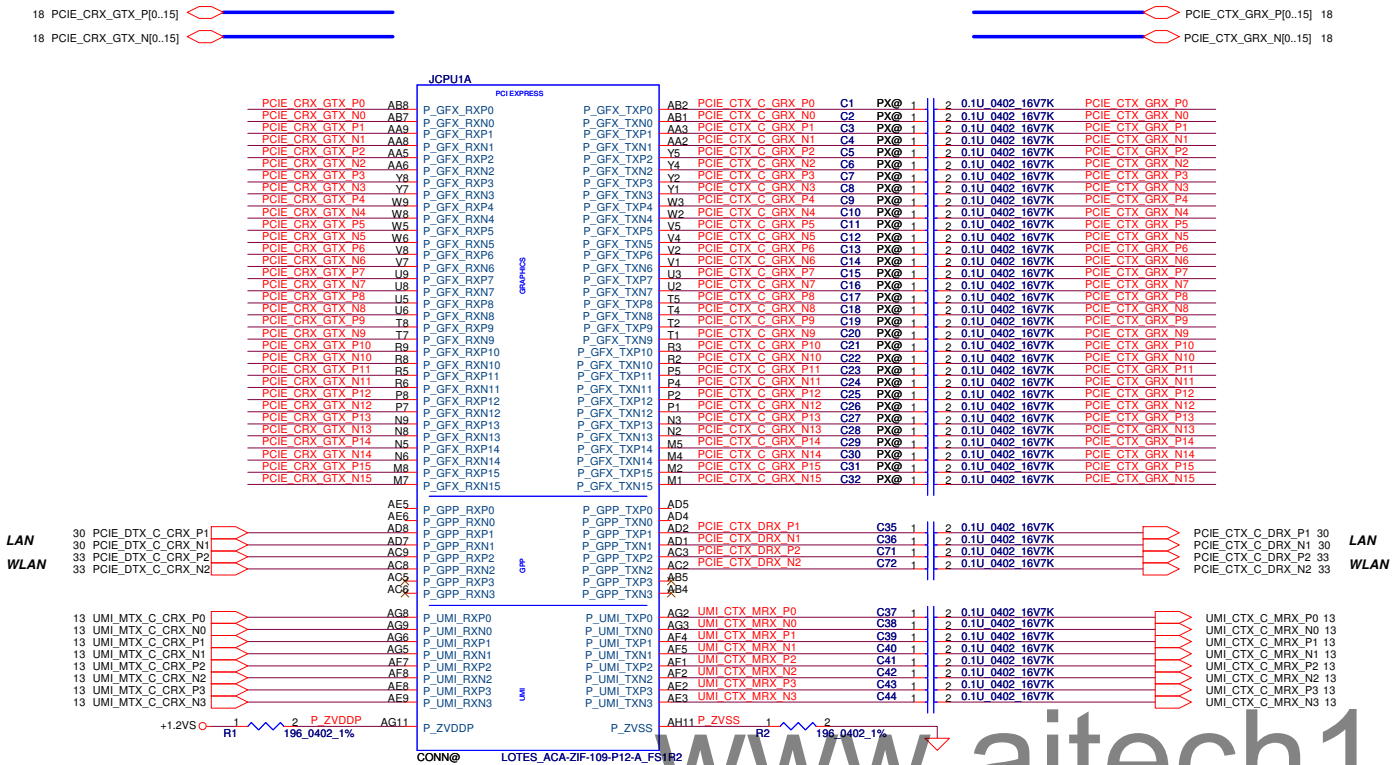

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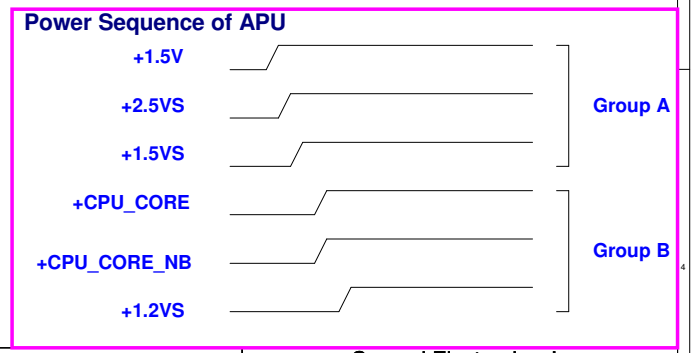

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Title: FS1r2 PCIE/UMI

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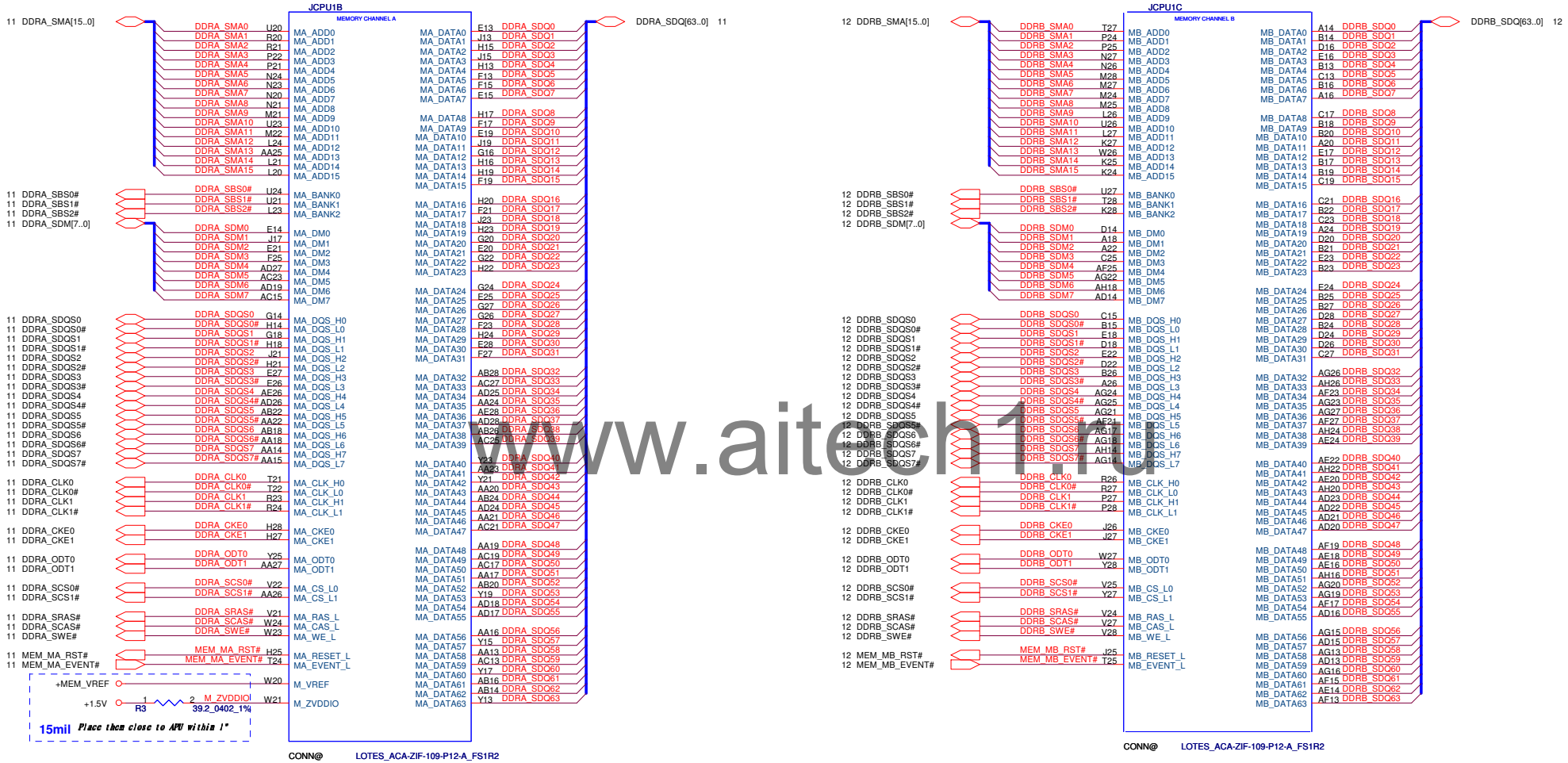

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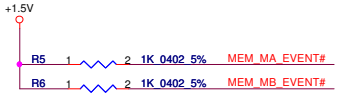
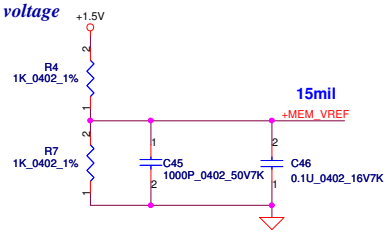
EVENT# pull high



0.75V reference voltage



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Compal Electronics, Inc.

Title: FS1r2 DDRIII Memory I/F

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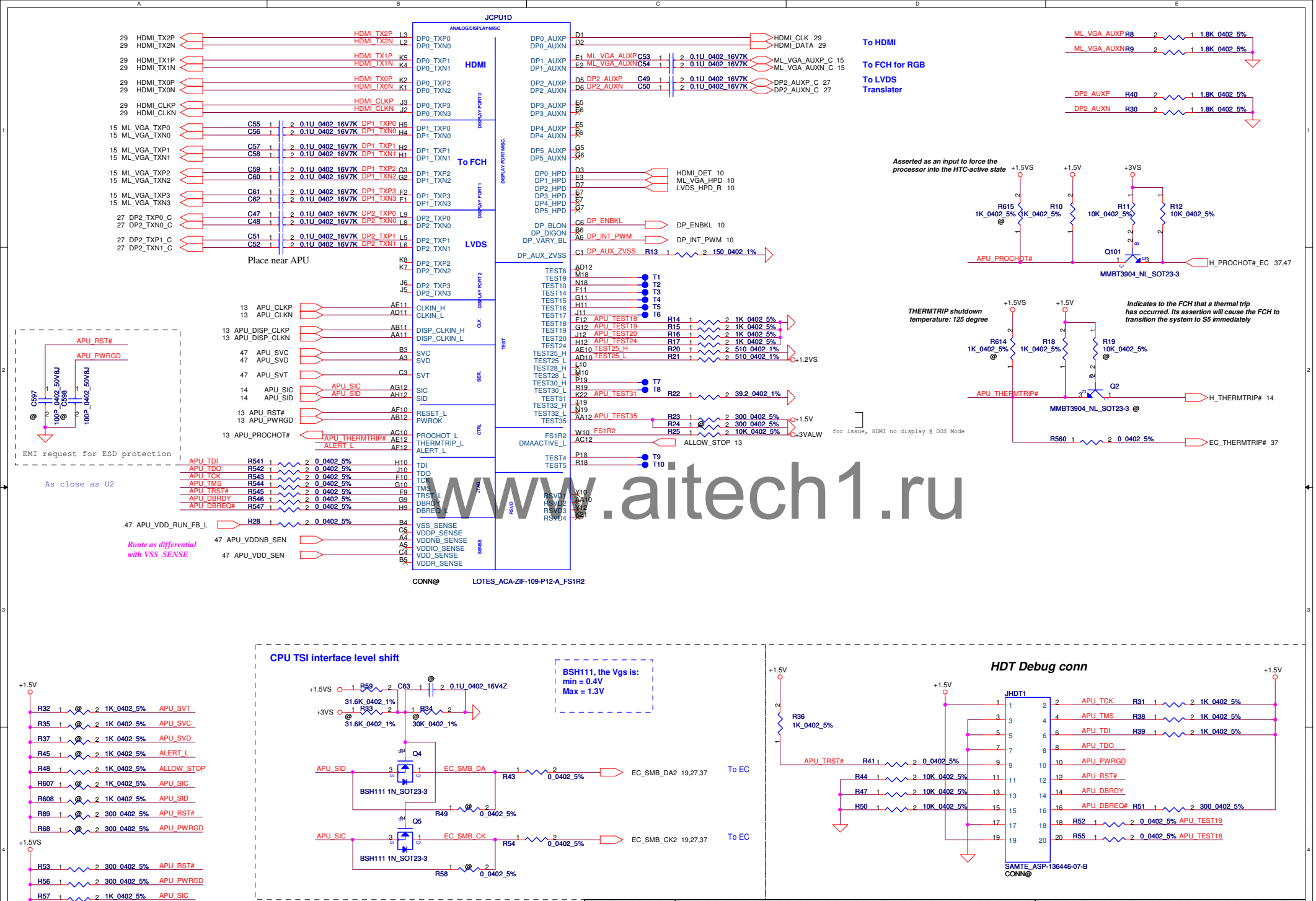

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Title: FS1r2 Display/MISC/HDT

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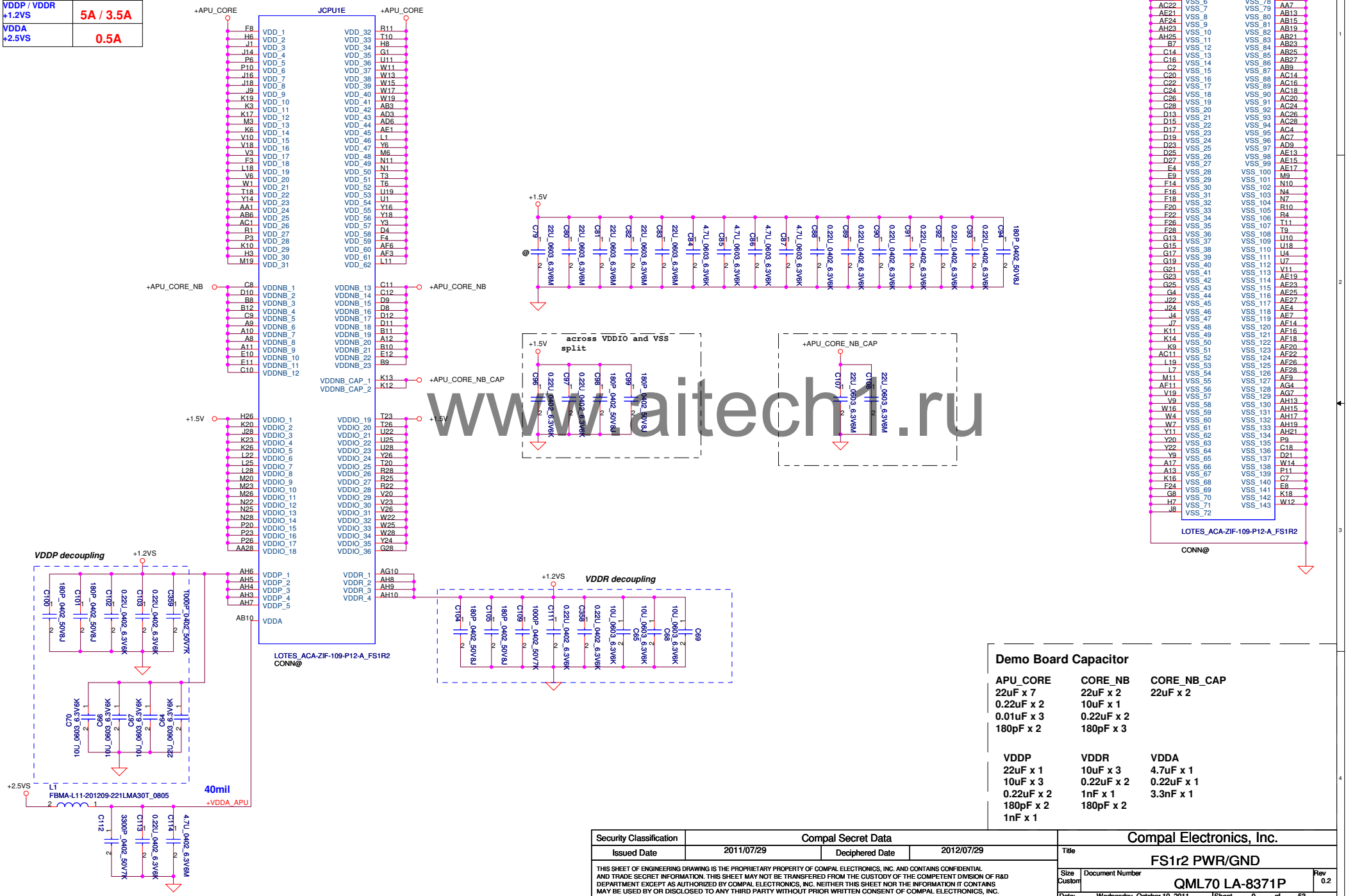
Power Name	Consumption
VDD +CPU_CORE	60A
VDDNB +CPU_CORE_NB	29A
VDDIO +1.5V	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.5A



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Demo Board Capacitor

APU_CORE	CORE_NB	CORE_NB_CAP
22uF x 7	22uF x 2	22uF x 2
0.22uF x 2	10uF x 1	
0.01uF x 3	0.22uF x 2	
180pF x 2	180pF x 3	

VDDP	VDDR	VDDA
22uF x 1	10uF x 3	4.7uF x 1
10uF x 3	0.22uF x 2	0.22uF x 1
0.22uF x 2	1nF x 1	3.3nF x 1
180pF x 2	180pF x 2	
1nF x 1		

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Title: FS1r2 PWR/GND

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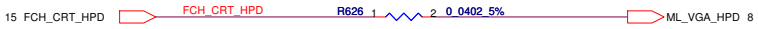
HPD

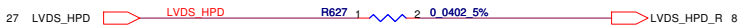
CRT HPD

From FCH



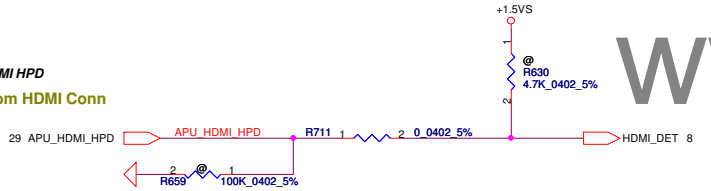
Translator HPD

From Translator

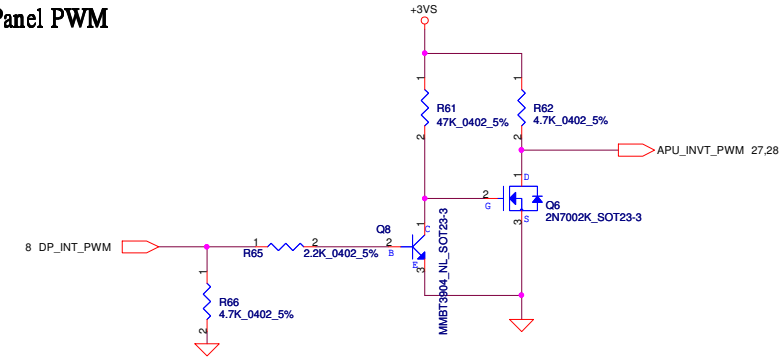


HDMI HPD

From HDMI Conn



Panel PWM



Panel ENBKL

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Title: FS1r2 Signal Level Shifter

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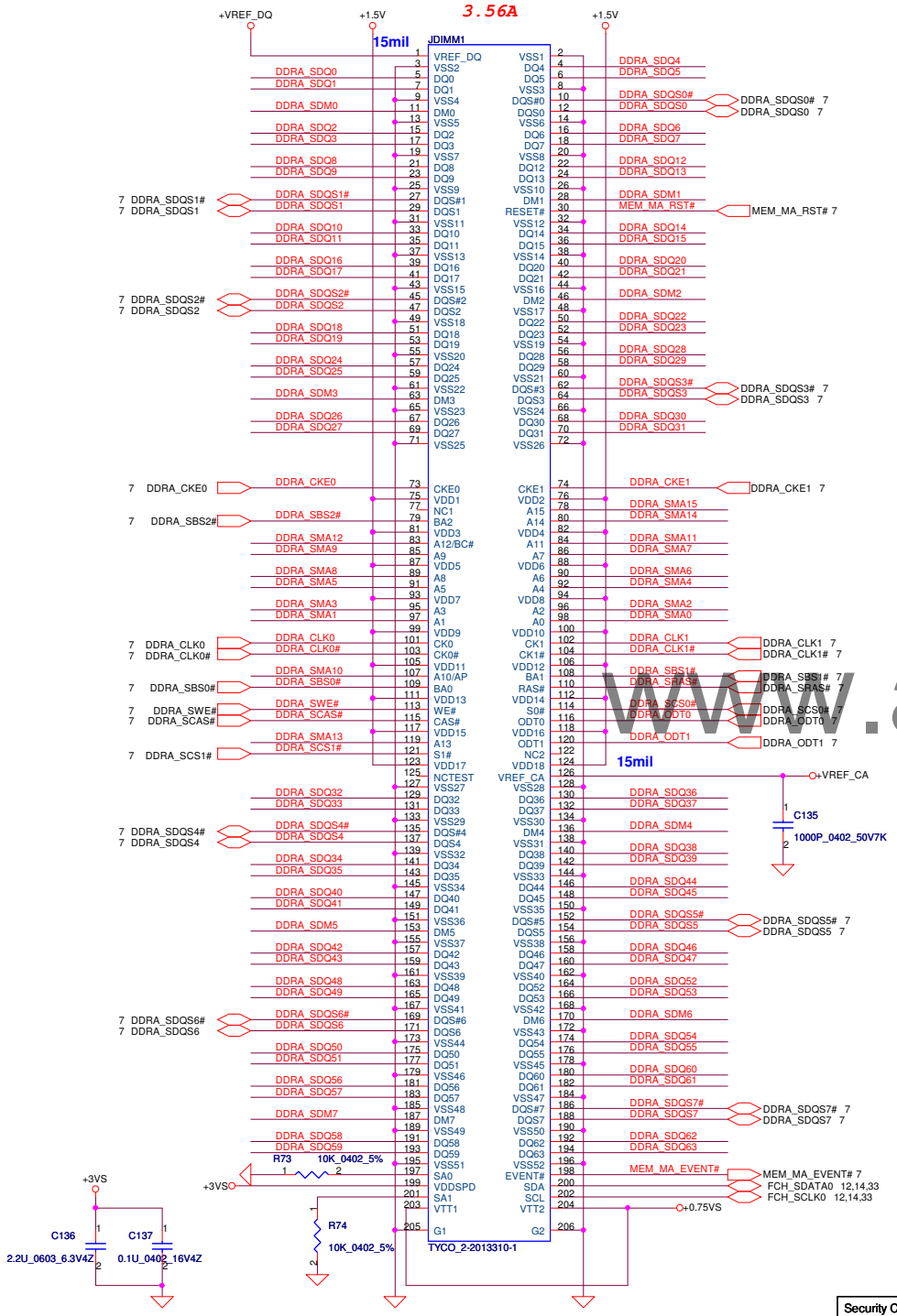

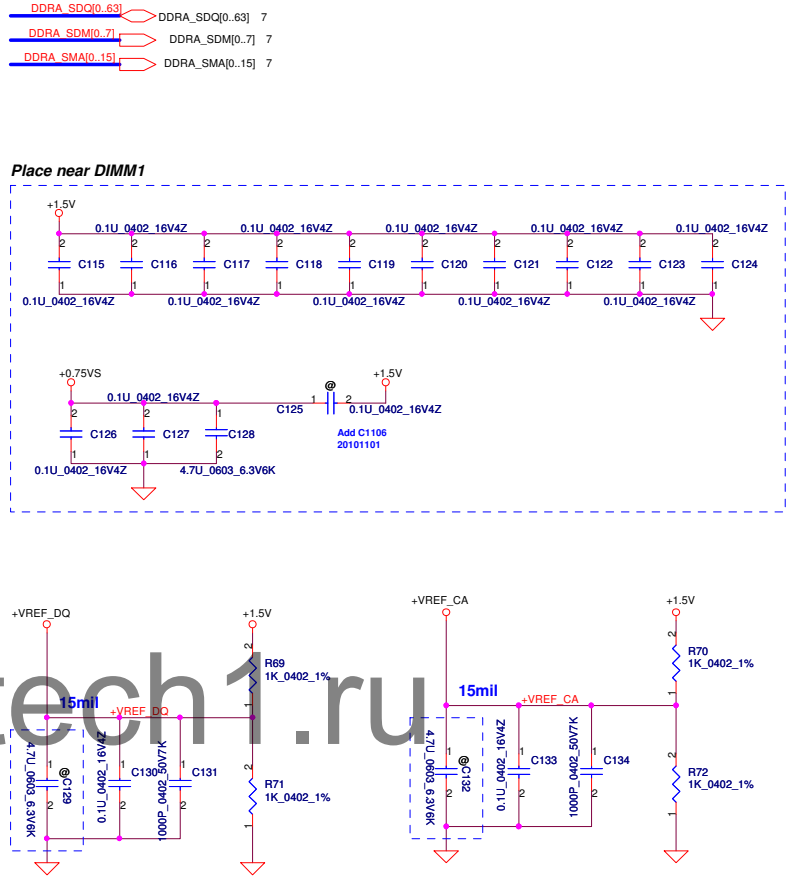

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Title: DDRIII SO-DIMM 1

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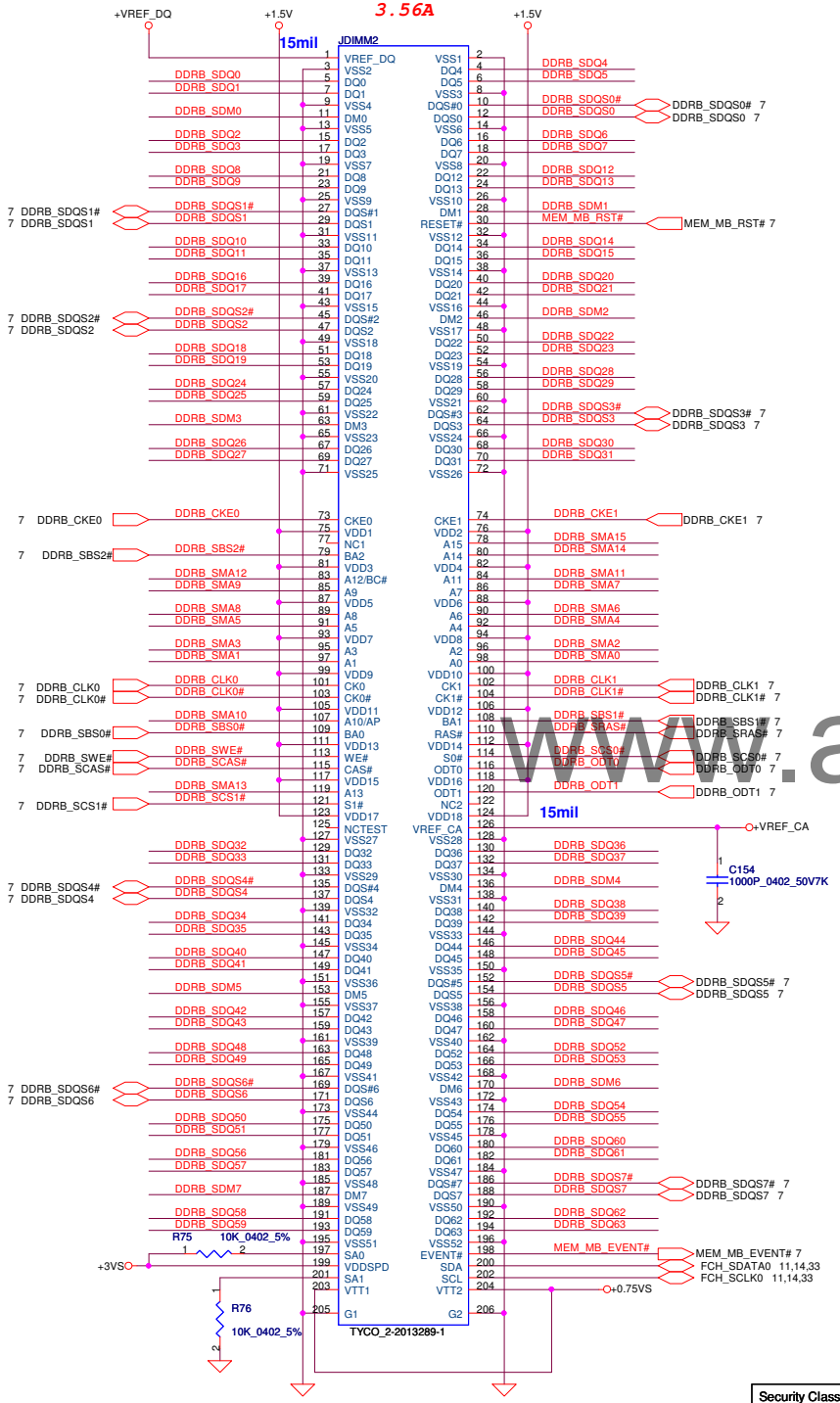

DIMM_B STD H:5.2mm

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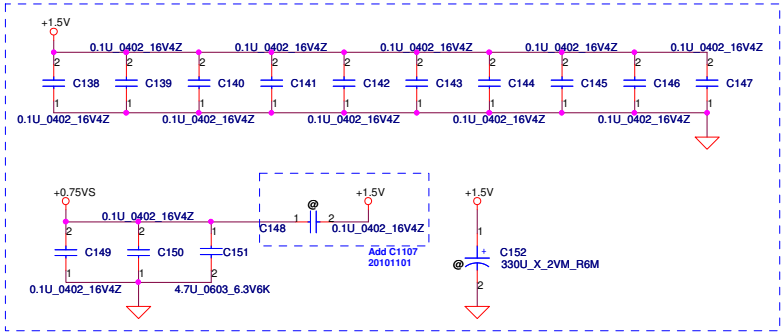
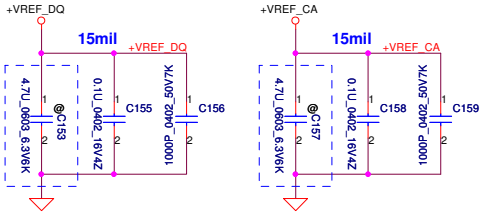
DDRB_SDQ[0..63] — DDRB_SDQ[0..63] 7

DDRB_SDM[0..7] — DDRB_SDM[0..7] 7

DDRB_SMA[0..15] — DDRB_SMA[0..15] 7

Place near DIMM2





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Title: DDRIII SO-DIMM 2

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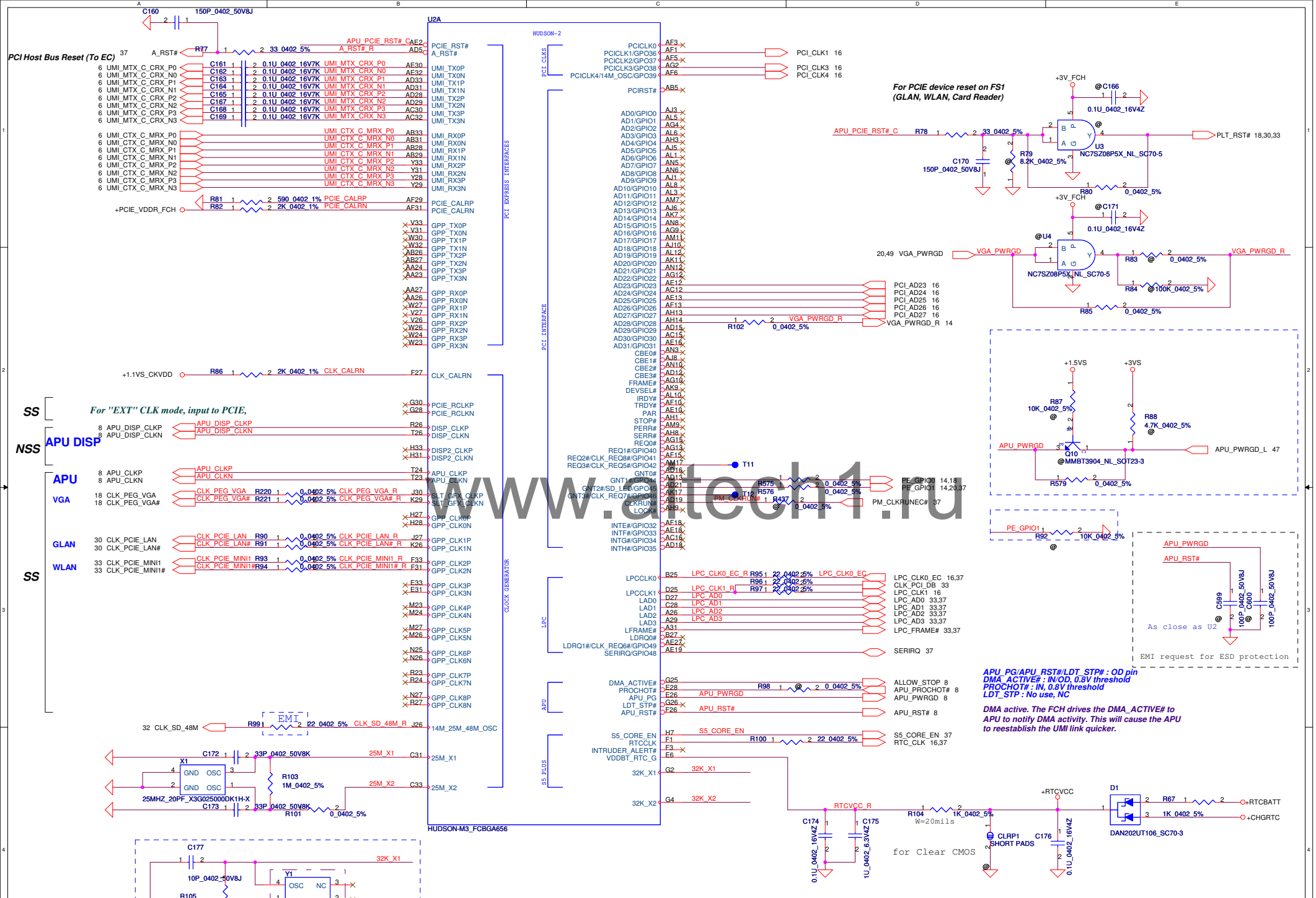

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Title: Hudson-M2/M3-UMI/PCI/CLOCK/LPC/RTC

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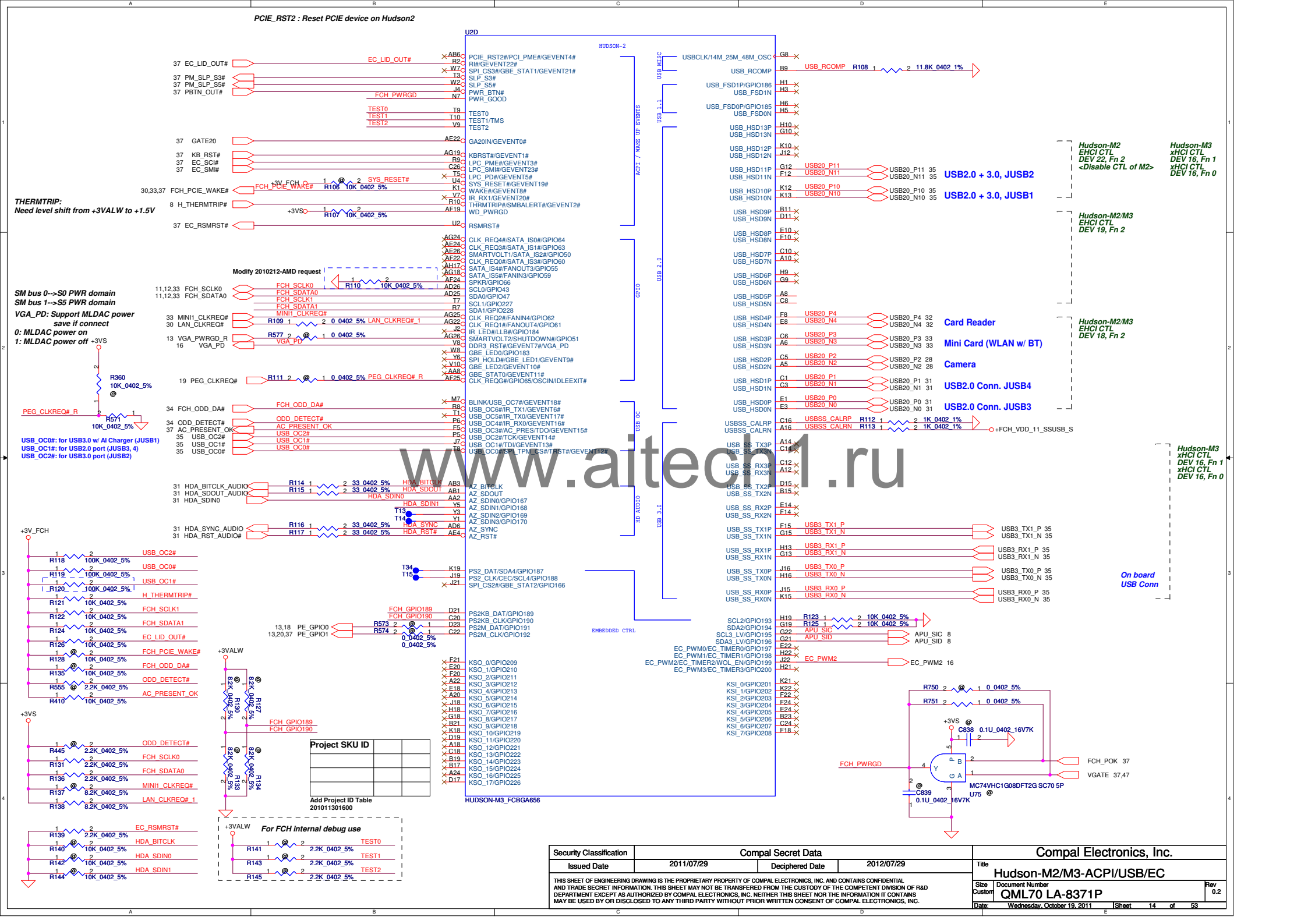

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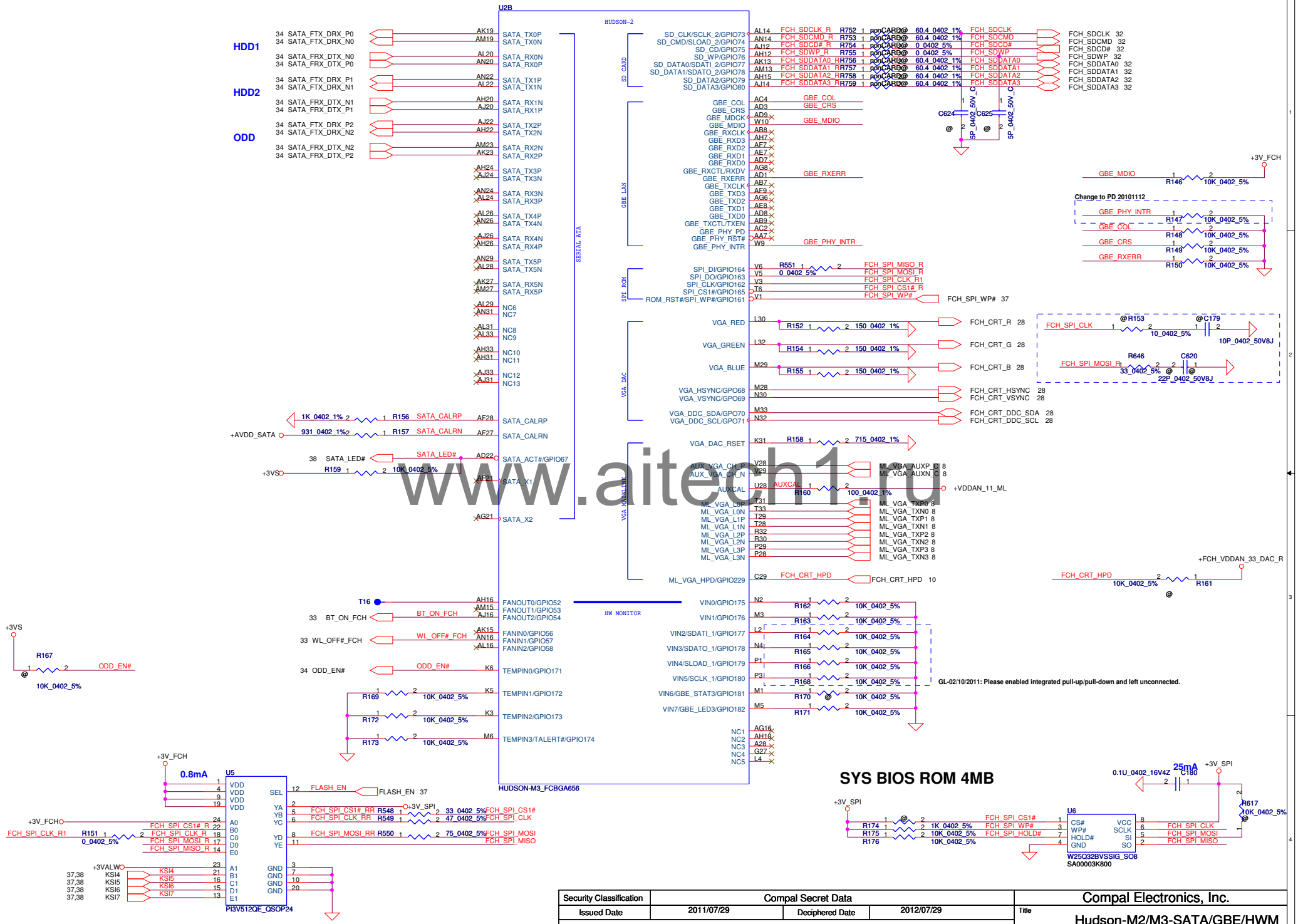

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Compal Electronics, Inc.

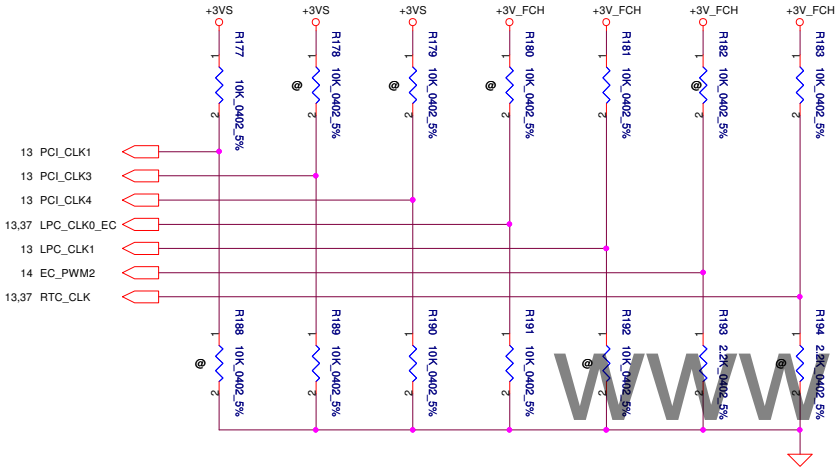
Title: Hudson-M2/M3-SATA/GBE/HWM

Size: Custom | Document Number: QML70 LA-8371P | Rev: 0.11

Date: Wednesday, October 19, 2011 | Sheet 15 of 53

STRAP PINS

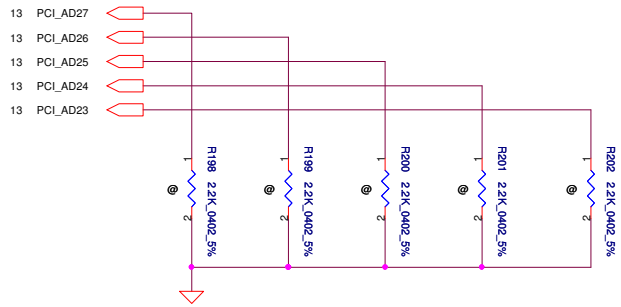
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM	S5 PLUS MODE ENABLED

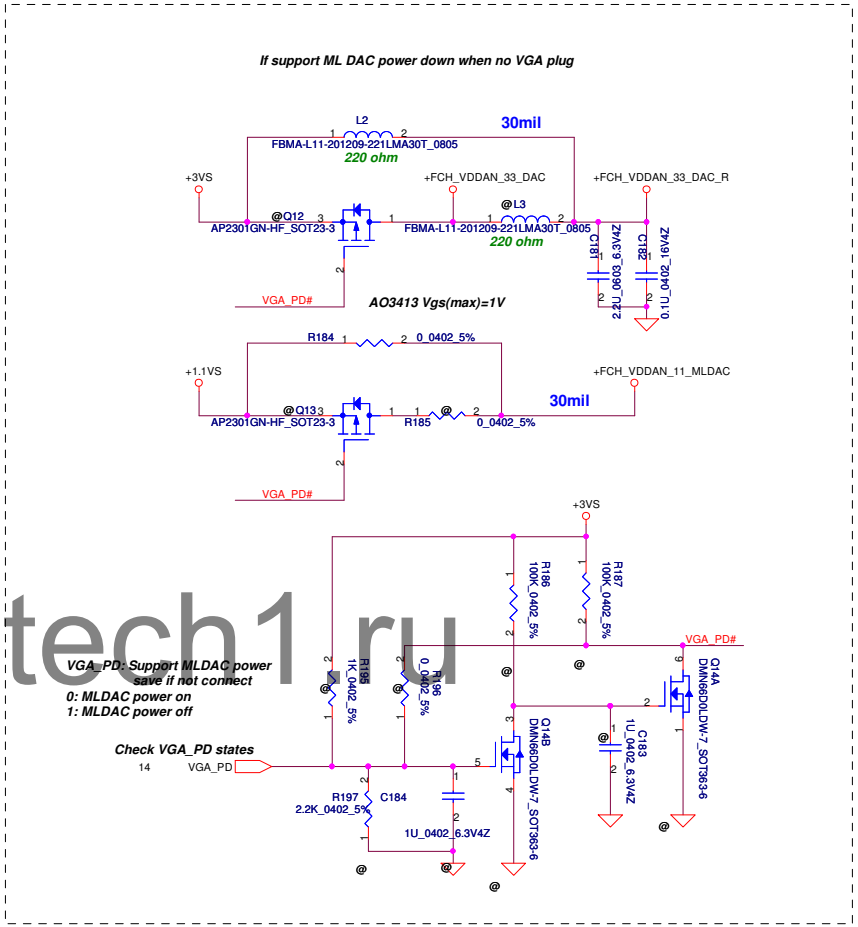


DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT





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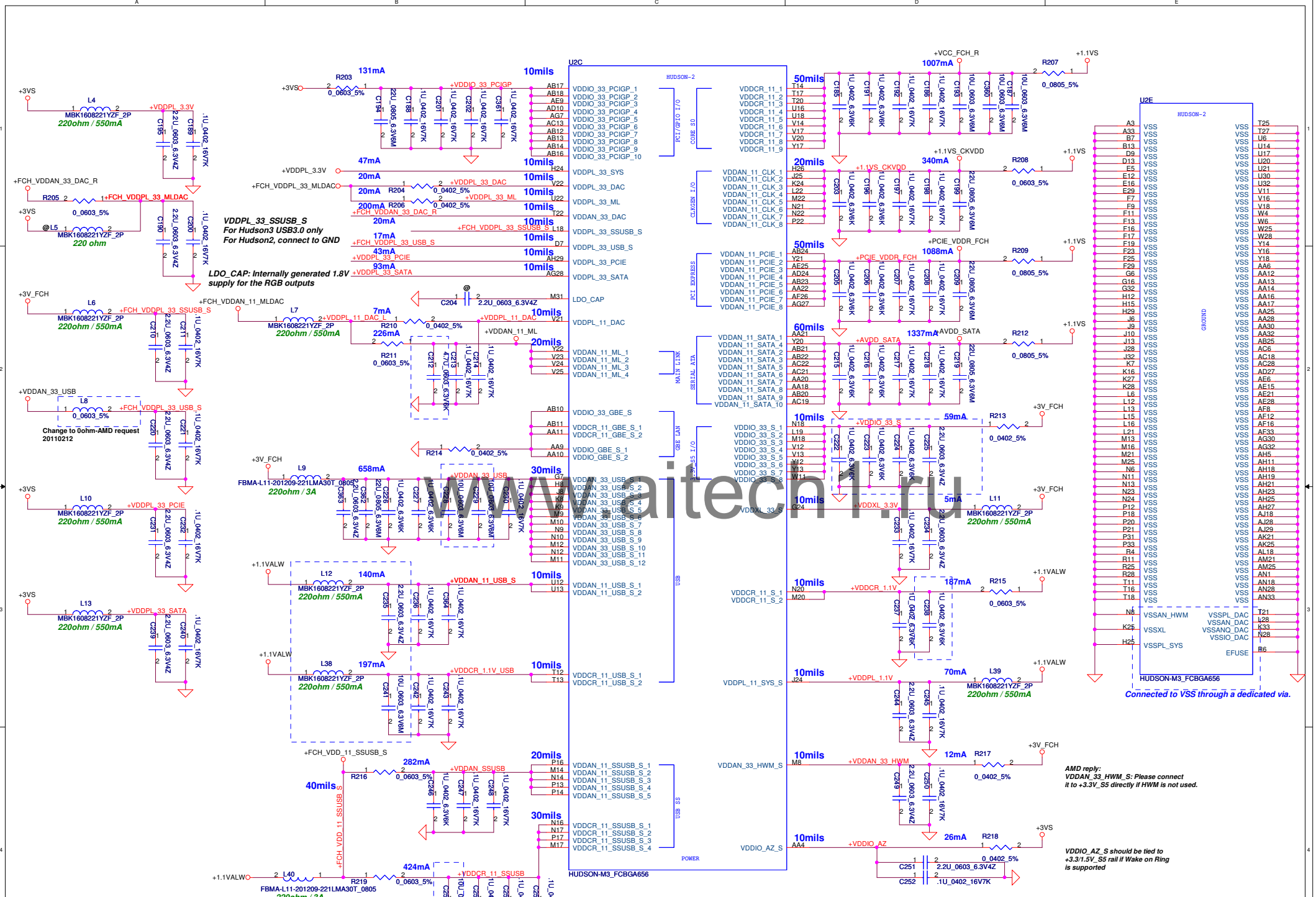
Compal Electronics, Inc.

Title: Hudson-M2/M3-STRAP

Size: Custom | Document Number: QML70 LA-8371P | Rev: 0.2

Date: Wednesday, October 19, 2011 | Sheet 16 of 53



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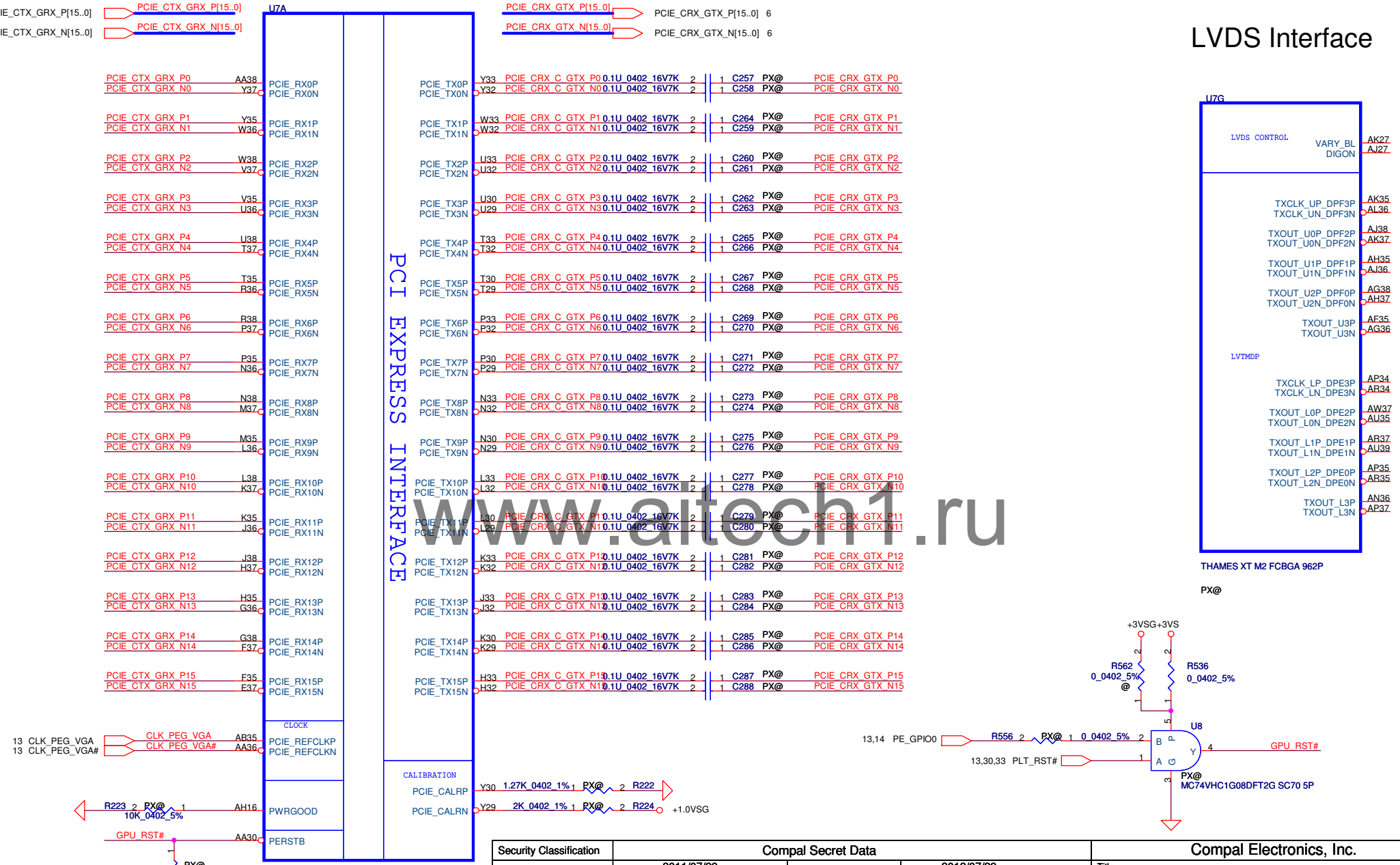
Compal Electronics, Inc.

Title: Hudson-M2/M3-POWER/GND

Size: Custom | Document Number: QML70 LA-8371P | Rev: 0.2

Date: Wednesday, October 19, 2011 | Sheet 17 of 53

LVDS Interface



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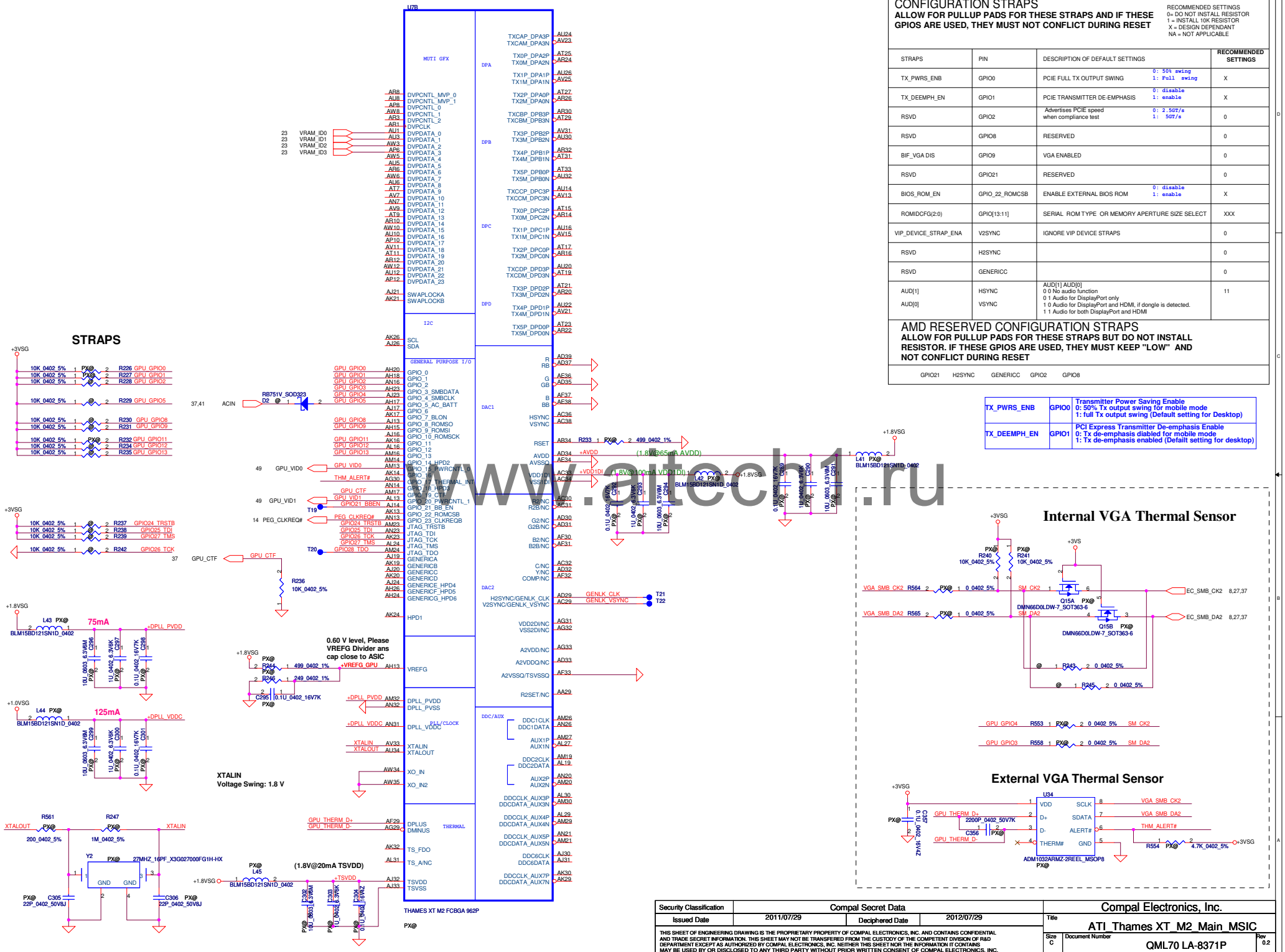
Compal Electronics, Inc.

Title: ATI_Thames XT_M2_PCIE/LVDS

Size: B | Document Number: QML70 LA-8371P | Rev: 0.2

Date: Wednesday, October 19, 2011 | Sheet 18 of 53



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0: 50% swing 1: Full swing	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS 0: disable 1: enable	X
RSVD	GPIO2	Advertises PCIE speed when compliance test 0: 2.5GT/s 1: 5GT/s	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0: disable 1: enable	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD	H2SYNC		0
RSVD	GENERICC		0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort only 1 0 Audio for DisplayPort and HDMI, if dongle is detected. 1 1 Audio for both DisplayPort and HDMI	11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21 H2SYNC GENERICC GPIO2 GPIO8

TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)

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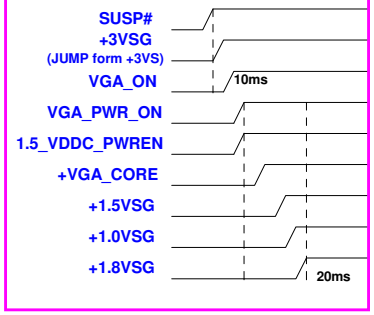
Title: ATI_Thames XT_M2_Main_MSIC

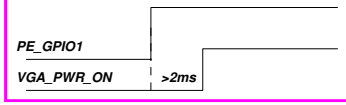
Size: C | Document Number: QML70 LA-8371P | Rev: 0.2

Date: Wednesday, October 19, 2011 | Sheet 19 of 53

Power Sequence of Whistler and Seymour

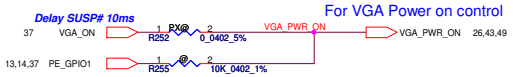


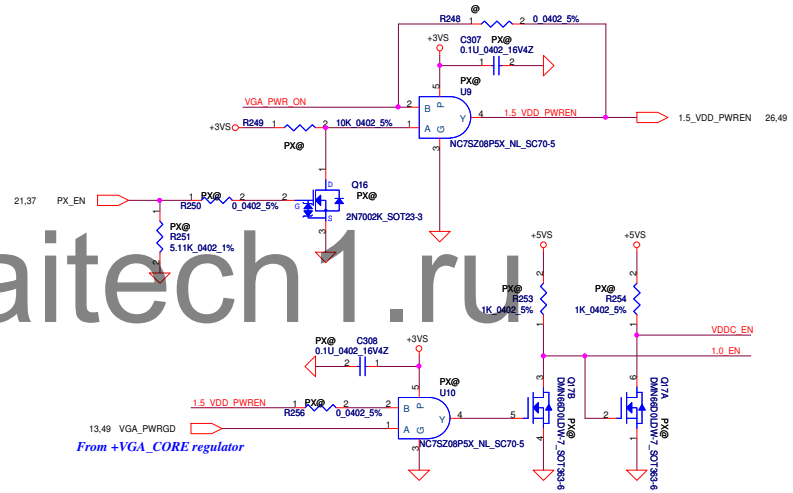
For PX sequence, >2mS delay is required between PE_GPIO1 and VGA_PWR_ON

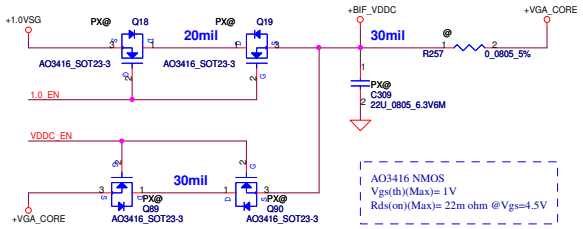


VGA Muxless with BACO Status Mapping table		
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

VGA Power Enable Signal Mapping table	
	Whislter
VGA_PWR_ON source signal	VGA_ON
+3.3VSG	SUSP#
+1.8VSG	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON
+VDDCI	Combine with +VGA_CORE
+VGA_CORE	1.5_VDDC_PWREN
+1.5VSG	1.5_VDDC_PWREN







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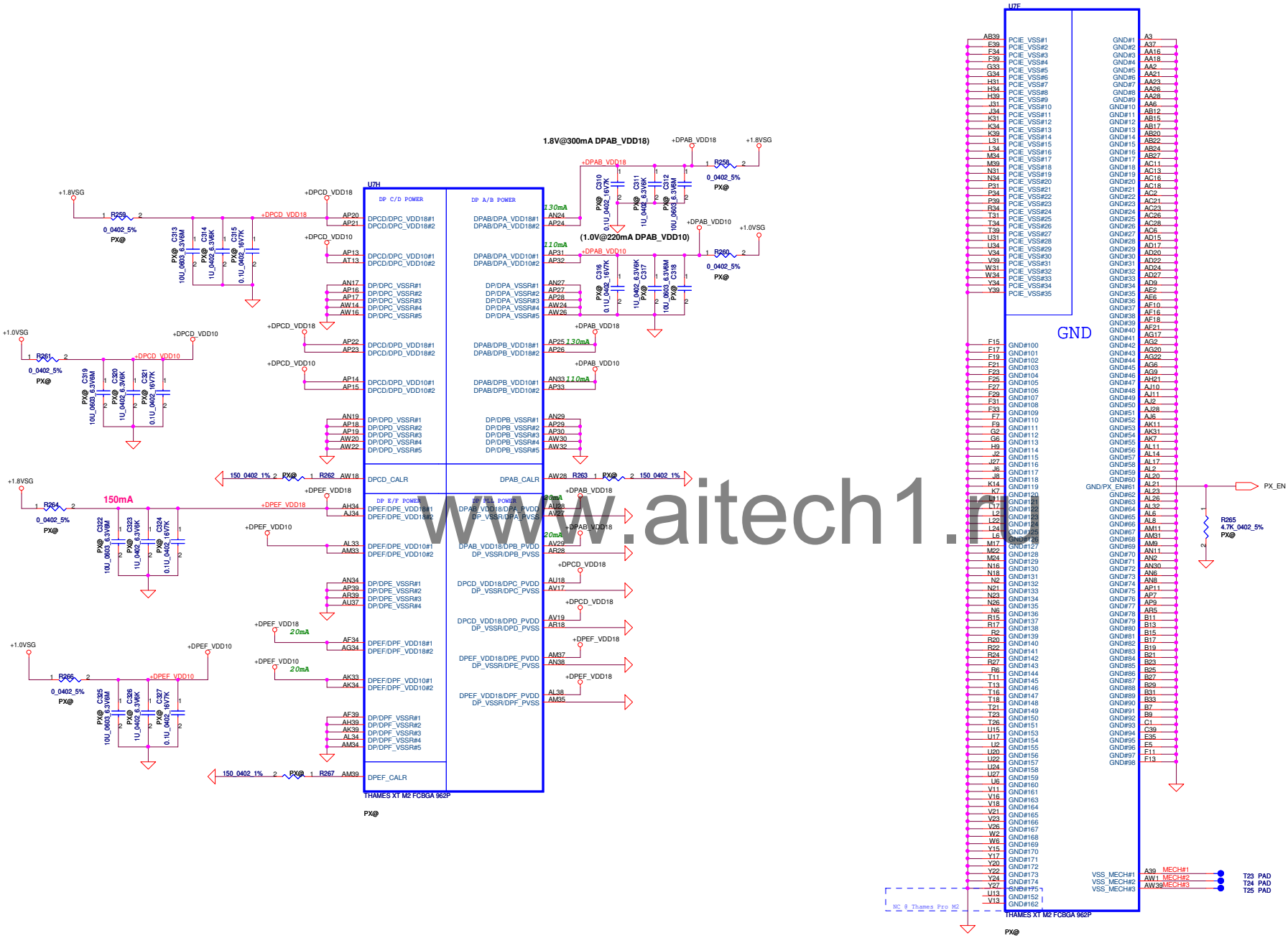
Title: ATI_Thames XT_M2_BACO POWER

Size: C | Document Number: QML70 LA-8371P | Rev: 0.2

Date: Wednesday, October 19, 2011 | Sheet 20 of 53



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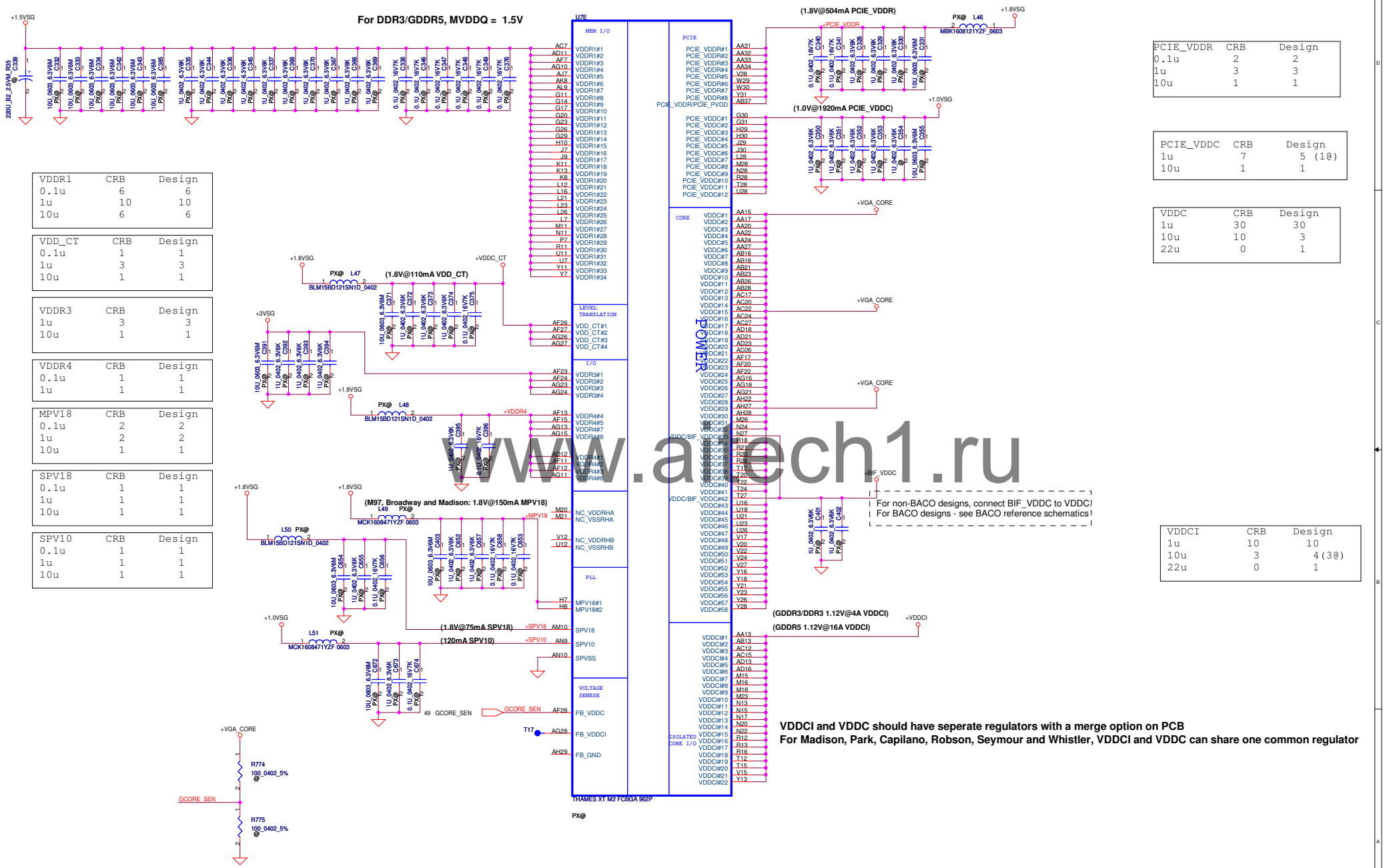
Title: ATI_Thames XT_M2_PWR_GND

Size: C | Document Number: QML70 LA-8371P | Rev: 0.2

Date: Wednesday, October 19, 2011 | Sheet 21 of 53



VDDR1	CRB	Design
0.1u	6	6
1u	10	10
10u	6	6

VDD_CT	CRB	Design
0.1u	1	1
1u	3	3
10u	1	1

VDDR3	CRB	Design
1u	3	3
10u	1	1

VDDR4	CRB	Design
0.1u	1	1
1u	1	1

MPV18	CRB	Design
0.1u	2	2
1u	2	2
10u	1	1

SPV18	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1

SPV10	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1

PCIE_VDDR	CRB	Design
0.1u	2	2
1u	3	3
10u	1	1

PCIE_VDDC	CRB	Design
1u	7	5 (1@)
10u	1	1

VDDC	CRB	Design
1u	30	30
10u	10	3
22u	0	1

VDDCI	CRB	Design
1u	10	10
10u	3	4(3@)
22u	0	1

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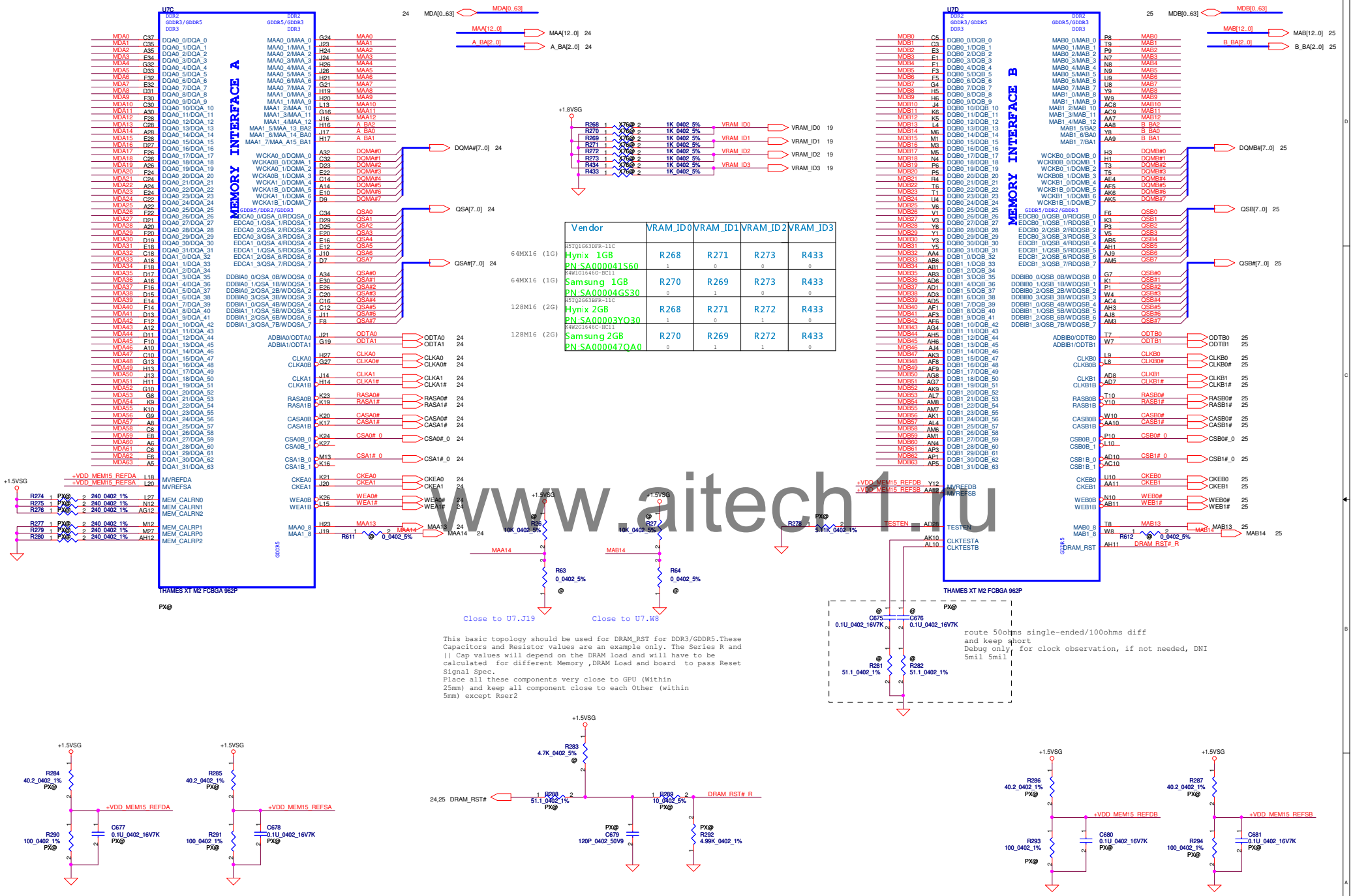
Title: ATI_Thames XT_M2_Power

Size: C | Document Number: QML70 LA-8371P | Rev: 0.2

Date: Wednesday, October 19, 2011 | Sheet 22 of 53



Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2	VRAM_ID3
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64MX16 (1G) K4W1G1646G-BC11 Samsung 1GB PN:SA00004GS30	R270 0	R269 1	R273 0	R433 0
128M16 (2G) H5TQ2G63BFR-11C Hynix 2GB PN:SA00003YO30	R268 1	R271 0	R272 1	R433 0
128M16 (2G) K4W2G1646C-HC11 Samsung 2GB PN:SA000047QA0	R270 0	R269 1	R272 1	R433 0

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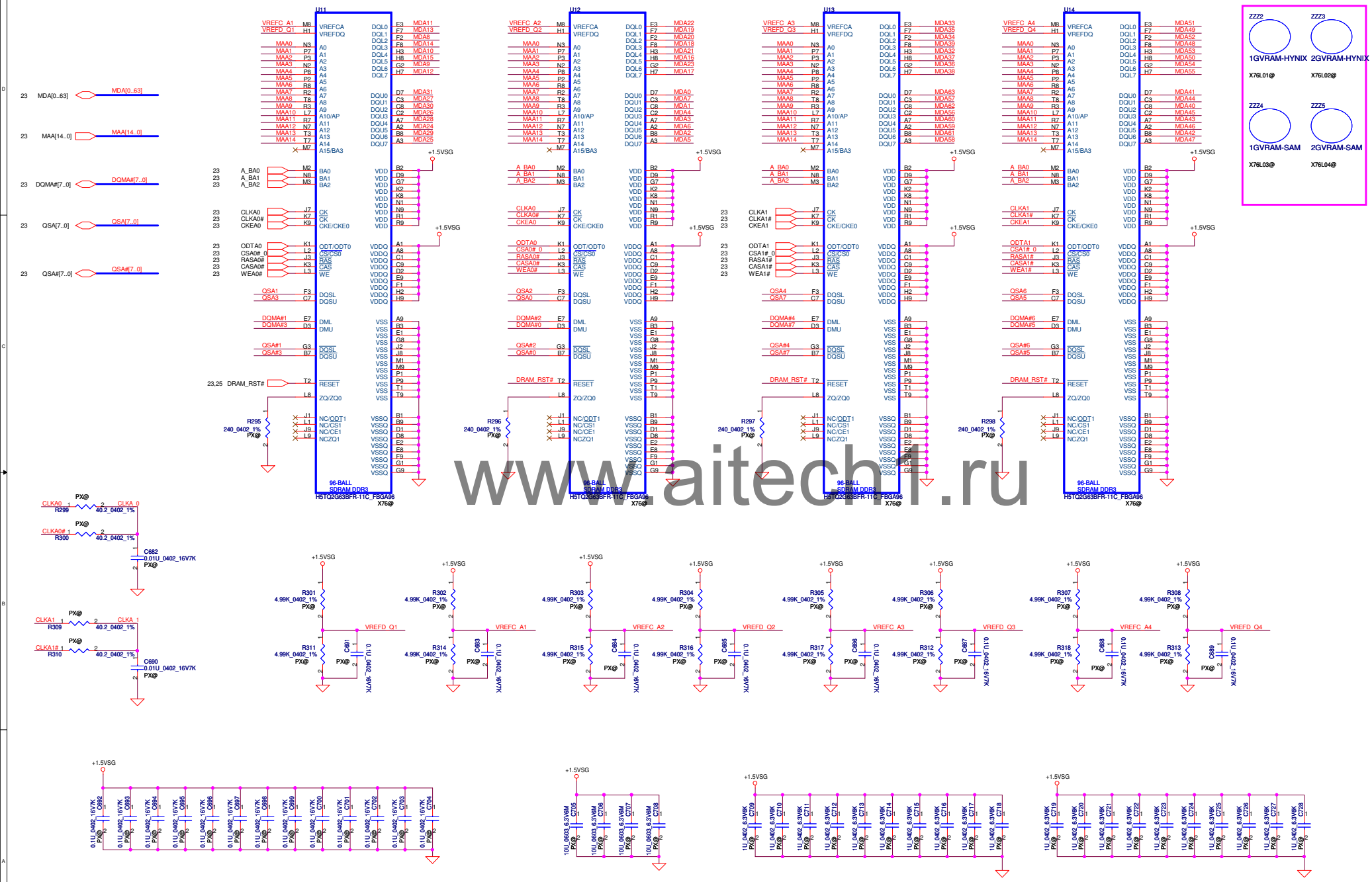
Compal Electronics, Inc.

Title: ATI_Thames XT_M2_MEM IF

Size: C | Document Number: QML70 LA-8371P | Rev: 0.2

Date: Wednesday, October 19, 2011 | Sheet 23 of 53



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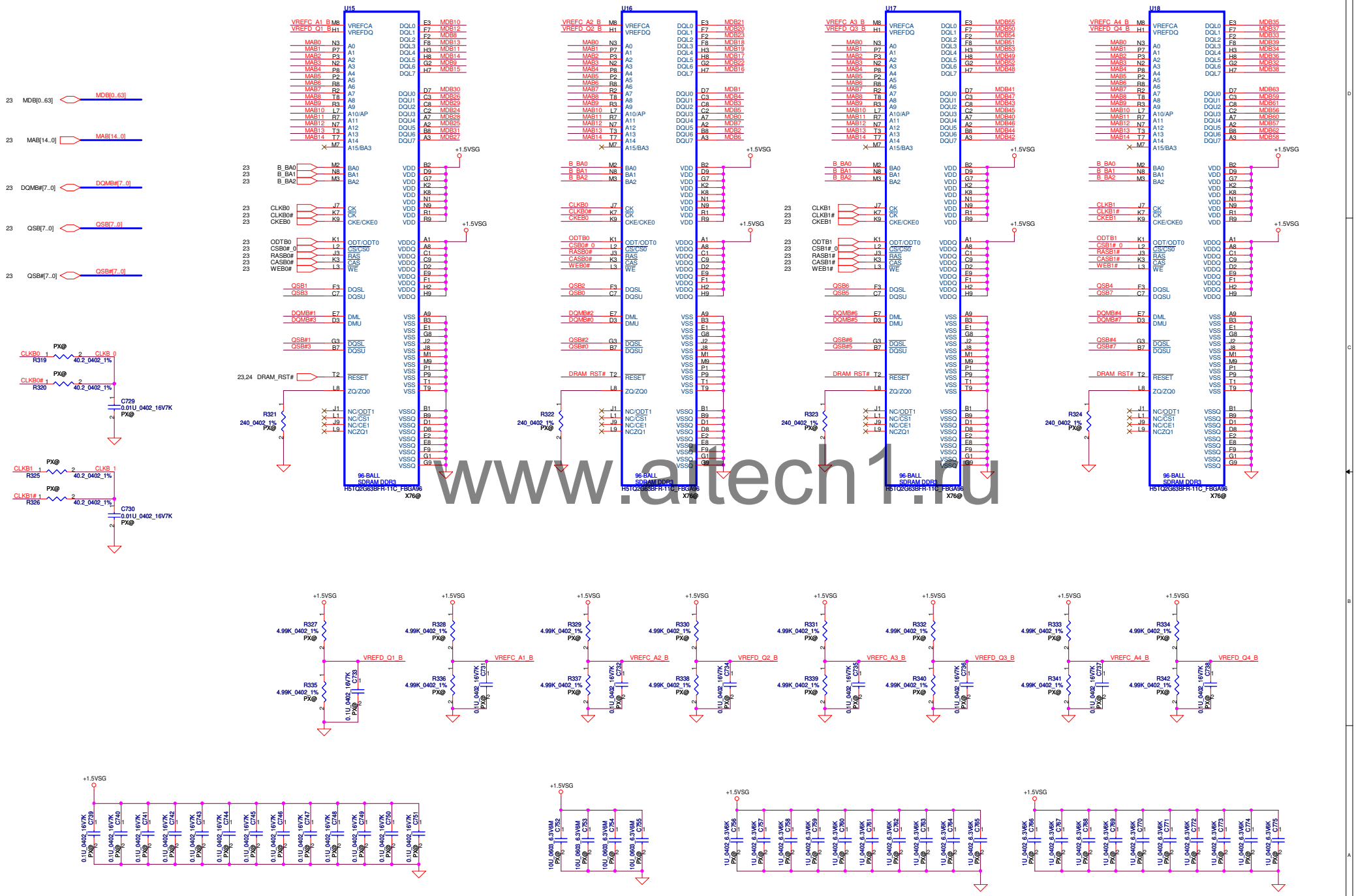
Compal Electronics, Inc.

Title: ATI_Thames XT_M2_VRAM_A

Size	Document Number	Rev
C	QML70 LA-8371P	0.2

Date: Wednesday, October 19, 2011 | Sheet 24 of 53



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Compal Electronics, Inc.

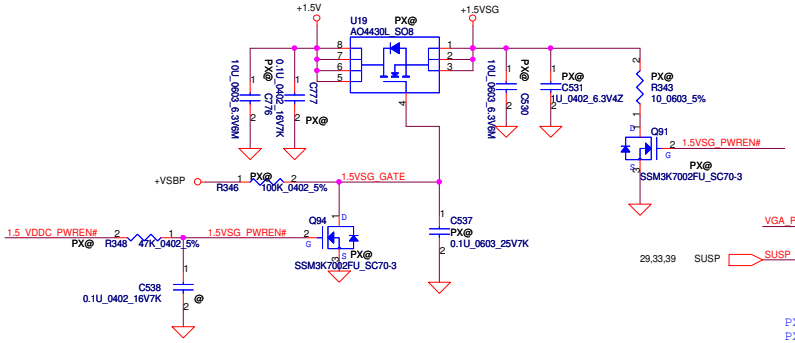
Title: ATI_Thames XT_M2_VRAM_B

Size	Document Number	Rev
C	QML70 LA-8371P	0.2

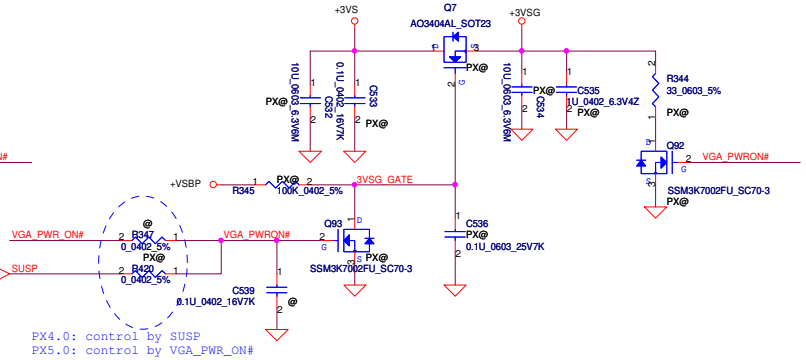
Date: Wednesday, October 19, 2011 | Sheet 25 of 53

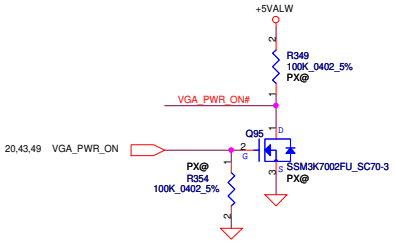
VGA Power

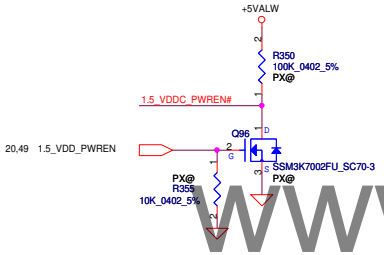
+1.5V to +1.5VSG (5.2A)

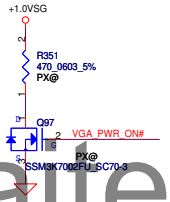


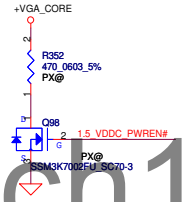
+3VS to +3VSG (60mA)

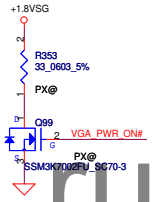












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Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

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Compal Electronics, Inc.

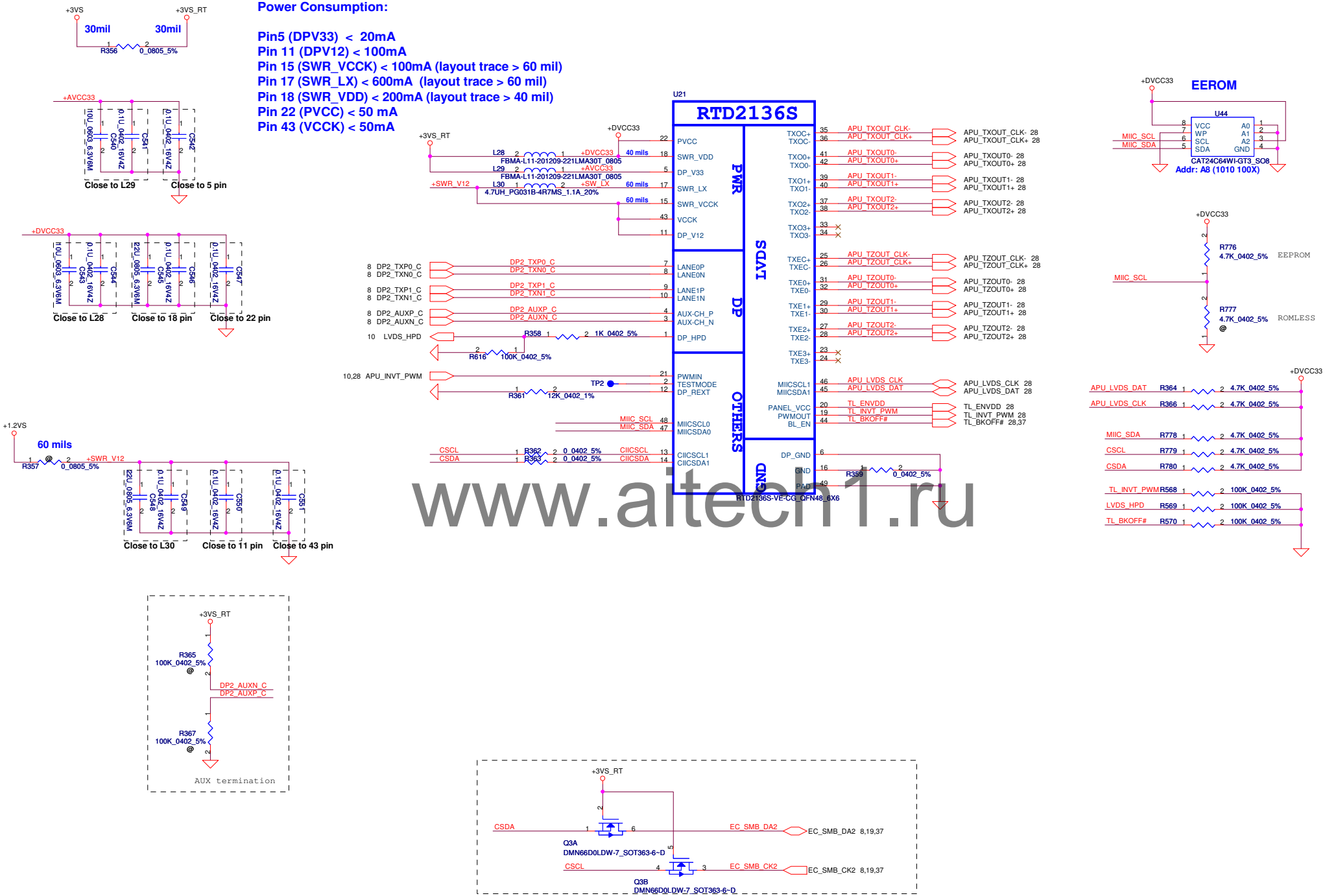
Title: **PCH (2/8) PCIE, SMBUS, CLK**

Size	Document Number	Rev
Custom	QML70 LA-8371P	0.2

Date: Wednesday, October 19, 2011 | Sheet 26 of 53

Power Consumption:

Pin5 (DPV33) < 20mA
Pin 11 (DPV12) < 100mA
Pin 15 (SWR_VCCK) < 100mA (layout trace > 60 mil)
Pin 17 (SWR_LX) < 600mA (layout trace > 60 mil)
Pin 18 (SWR_VDD) < 200mA (layout trace > 40 mil)
Pin 22 (PVCC) < 50 mA
Pin 43 (VCCK) < 50mA



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Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/07/29	Deciphered Date	2012/07/29	Title: LVDS Translator - RTD2132S
				Size: Custom; Document Number: QML70 LA-8371P; Rev: 0.11
				Date: Wednesday, October 19, 2011; Sheet 27 of 53

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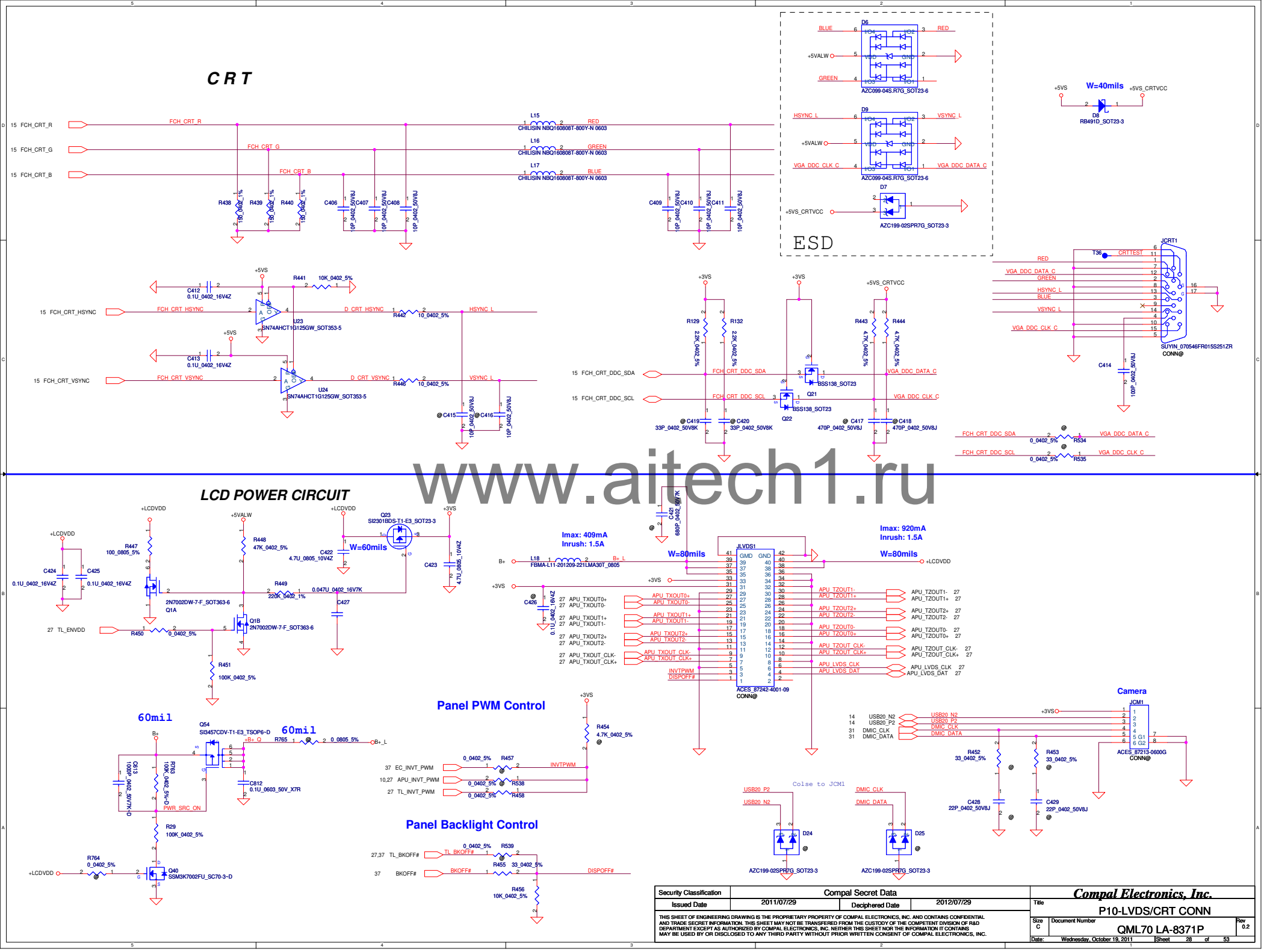

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Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

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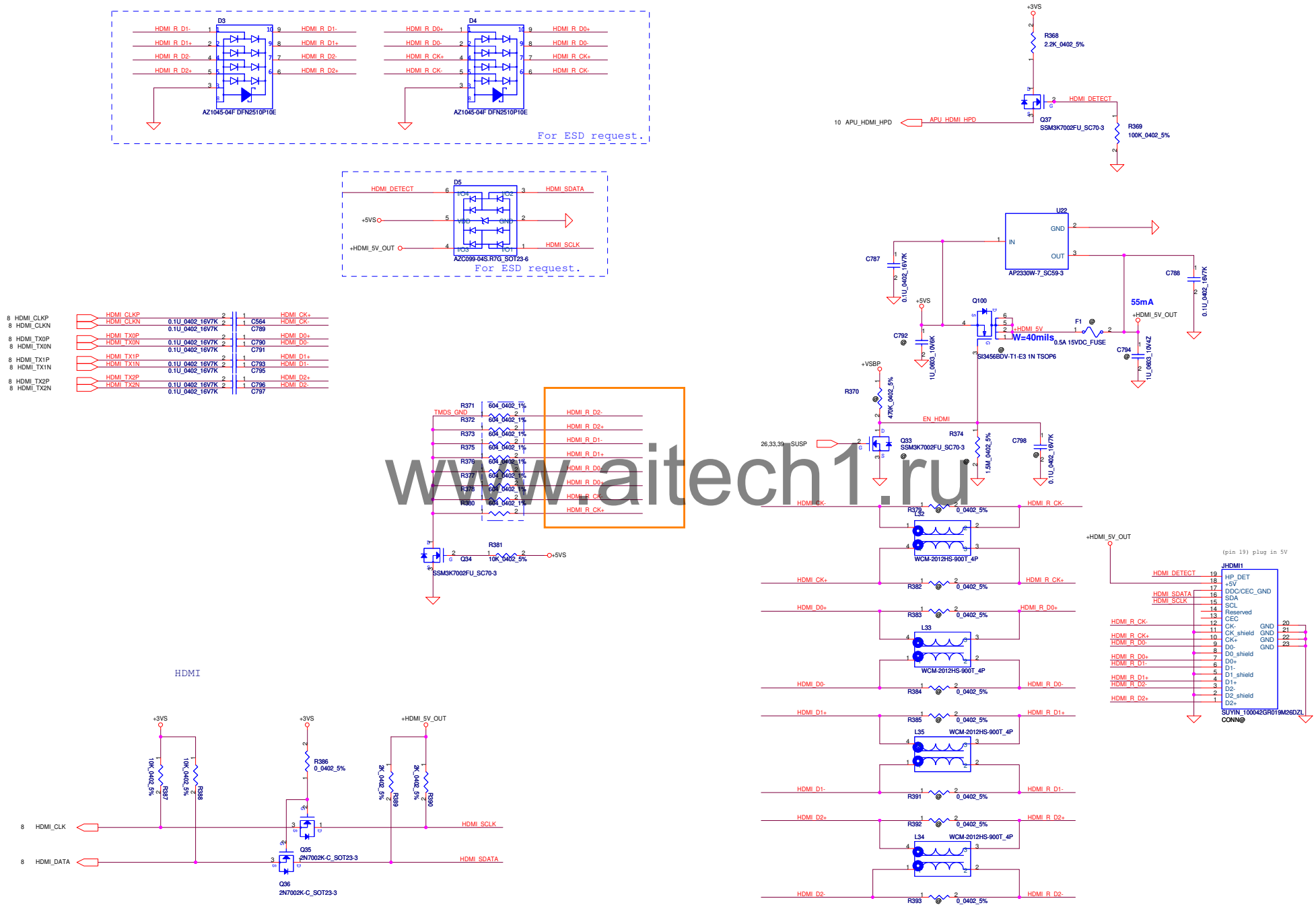
Compal Electronics, Inc.

Title: P10-LVDS/CRT CONN

Size: C | Document Number: QML70 LA-8371P | Rev: 0.2

Date: Wednesday, October 19, 2011 | Sheet 28 of 53



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Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

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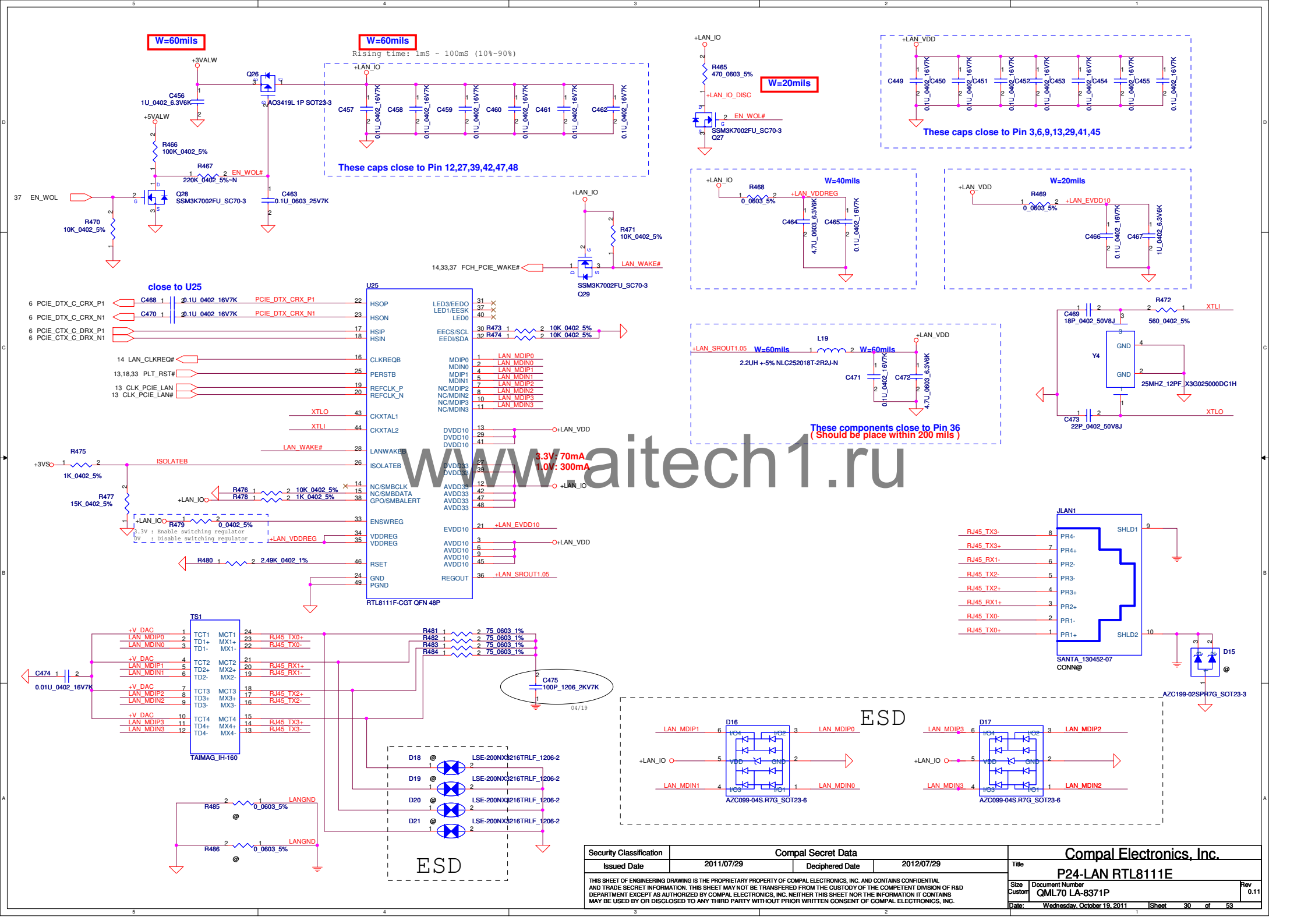
Compal Electronics, Inc.

Title: HDMI Connector

Size: C | Document Number: QML70 LA-8371P | Rev: 0.2

Date: Wednesday, October 19, 2011 | Sheet 29 of 53



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Issued Date	2011/07/29	Deciphered Date	2012/07/29

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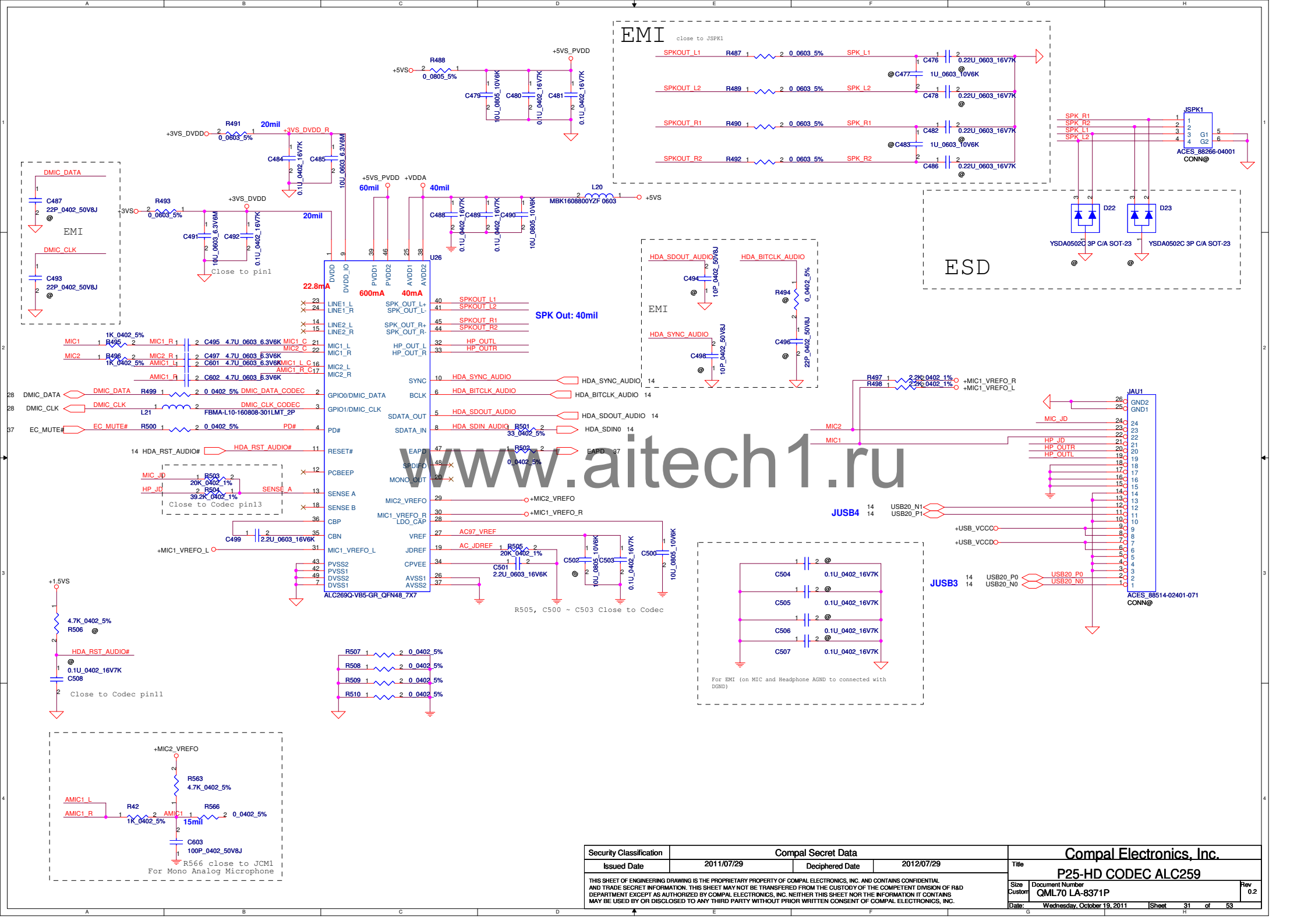
Compal Electronics, Inc.

Title: P24-LAN RTL8111E

Size: Custom | Document Number: QML70 LA-8371P | Rev: 0.11

Date: Wednesday, October 19, 2011 | Sheet 30 of 53



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Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

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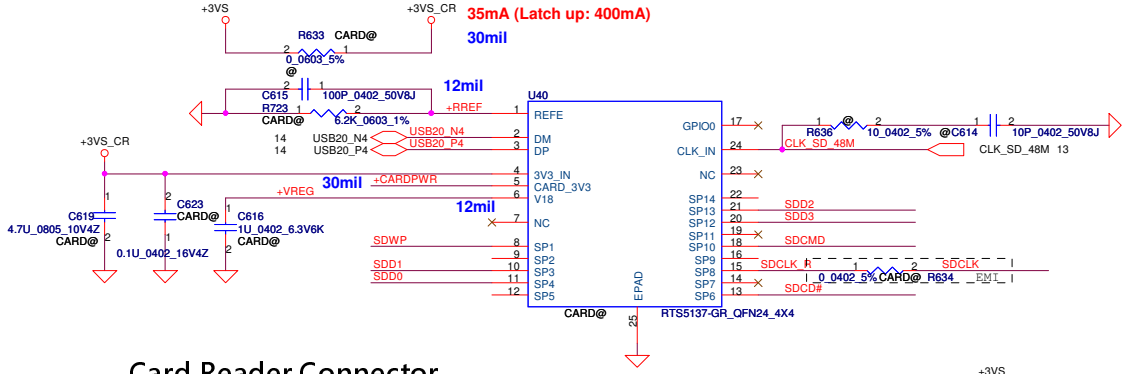
Compal Electronics, Inc.

Title: P25-HD CODEC ALC259

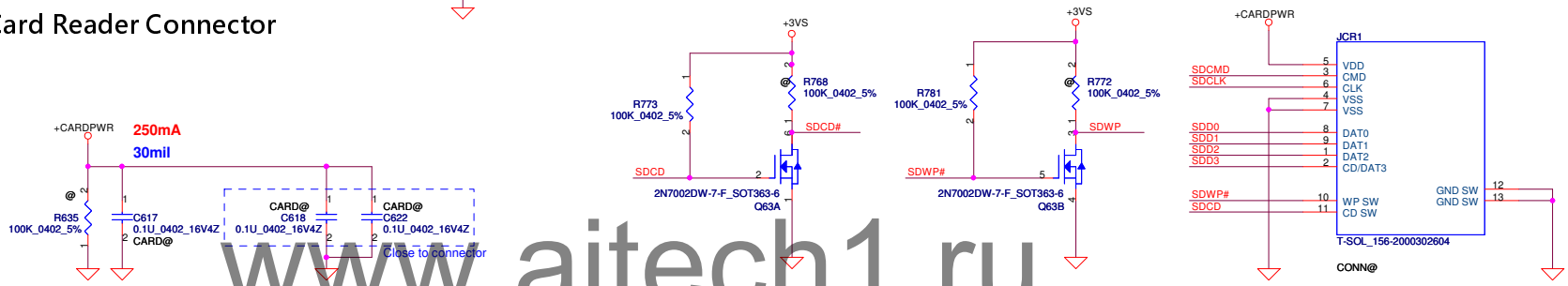
Size: Custom | Document Number: QML70 LA-8371P | Rev: 0.2

Date: Wednesday, October 19, 2011 | Sheet 31 of 53

Card Reader RTS5137
(only SD/MMC/MS function)



Card Reader Connector



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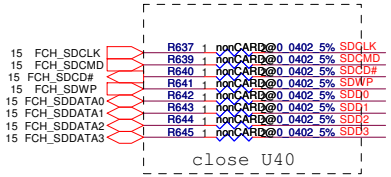

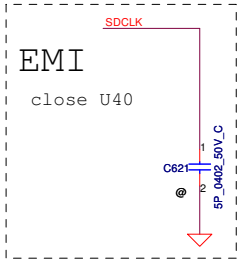

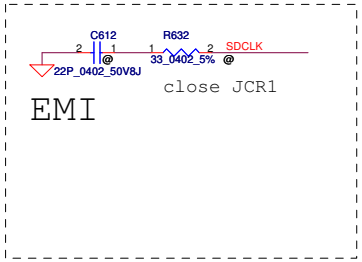

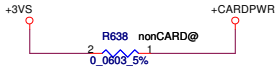

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/07/29	Deciphered Date	2012/07/29	Title: P26-RTS5137 Media Card Controller
				Size: Custom; Document Number: QML70 LA-8371P; Rev: 0.11
				Date: Wednesday, October 19, 2011; Sheet 32 of 53

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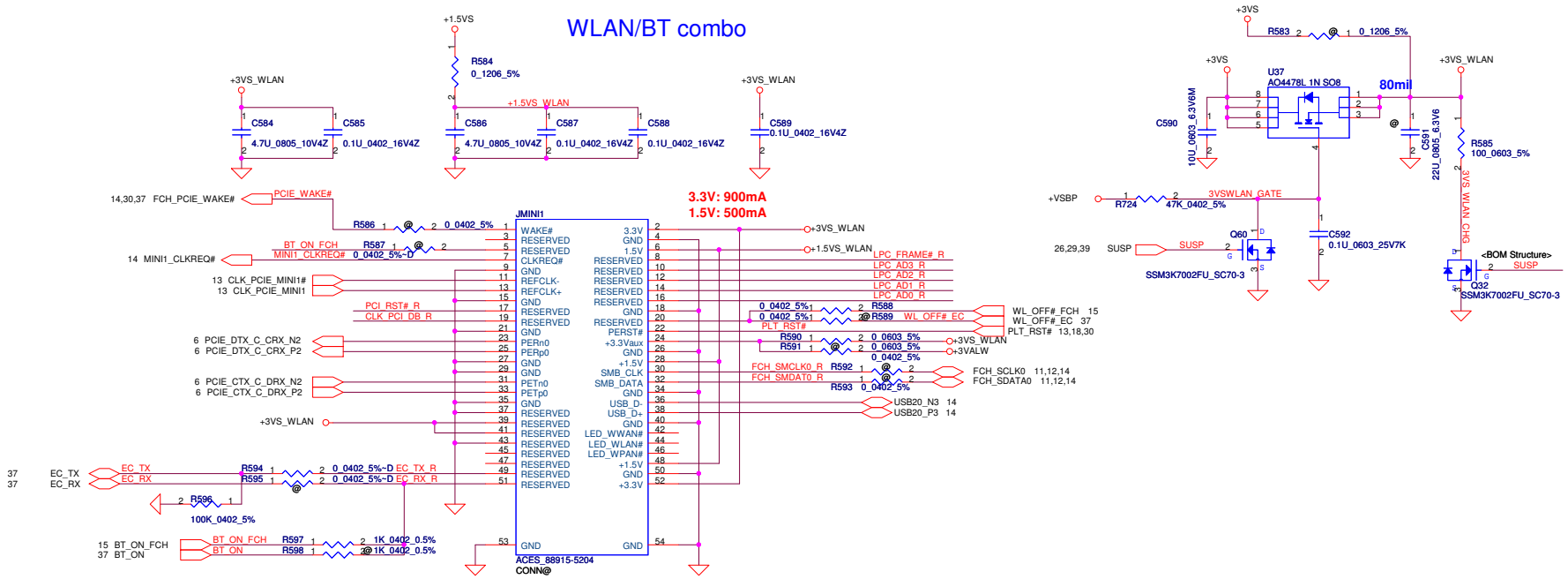
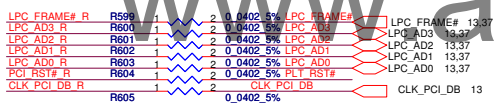
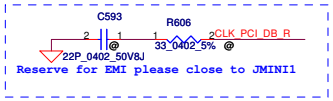
WLAN/BT combo



5.2 mm High

Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.





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Issued Date	2011/07/29	Deciphered Date	2012/07/29

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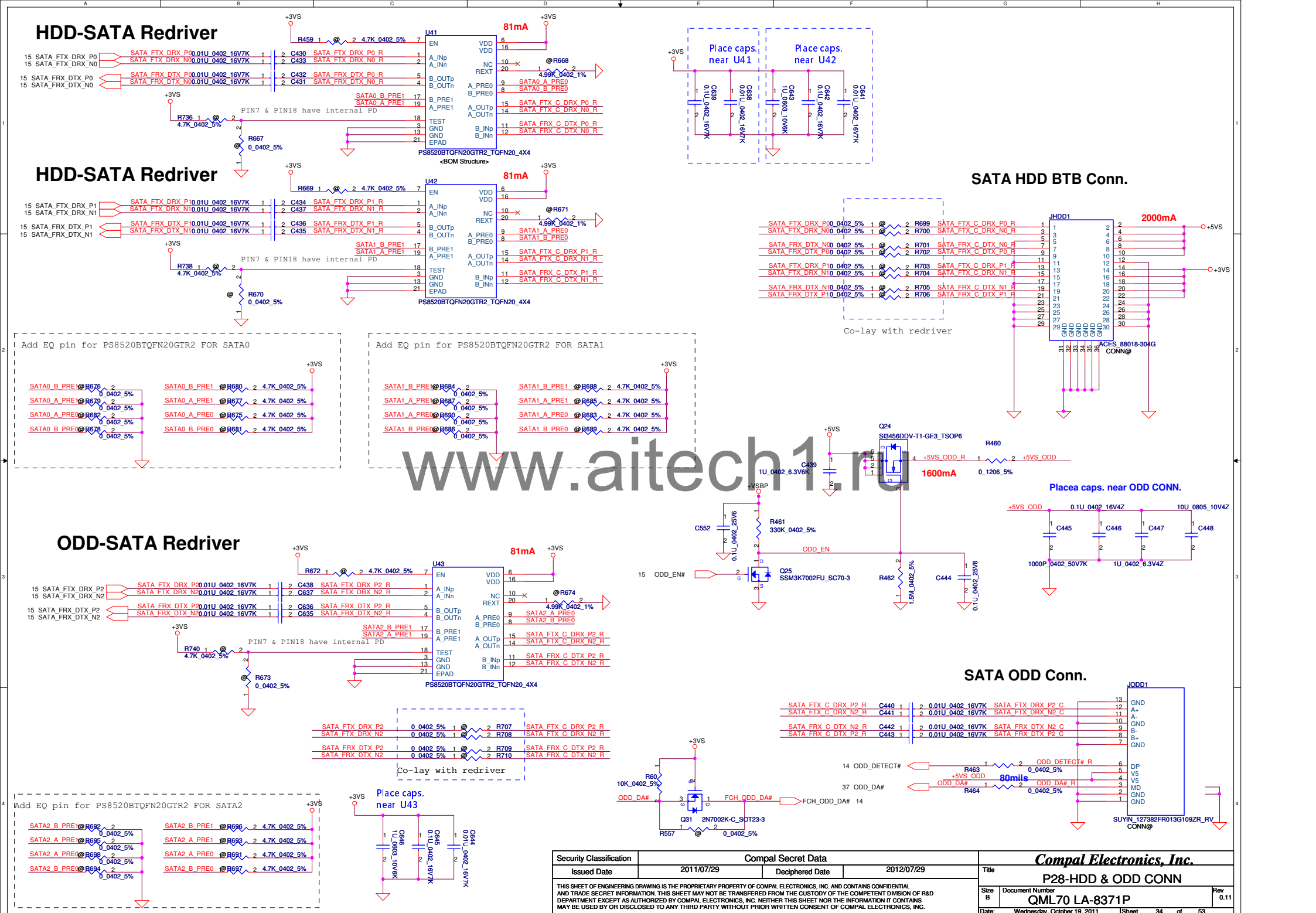
Compal Electronics, Inc.

Title: WLAN/ WWAN/ m-SATA

Size: Custom | Document Number: QML70 LA-8371P | Rev: 0.2

Date: Wednesday, October 19, 2011 | Sheet 33 of 53



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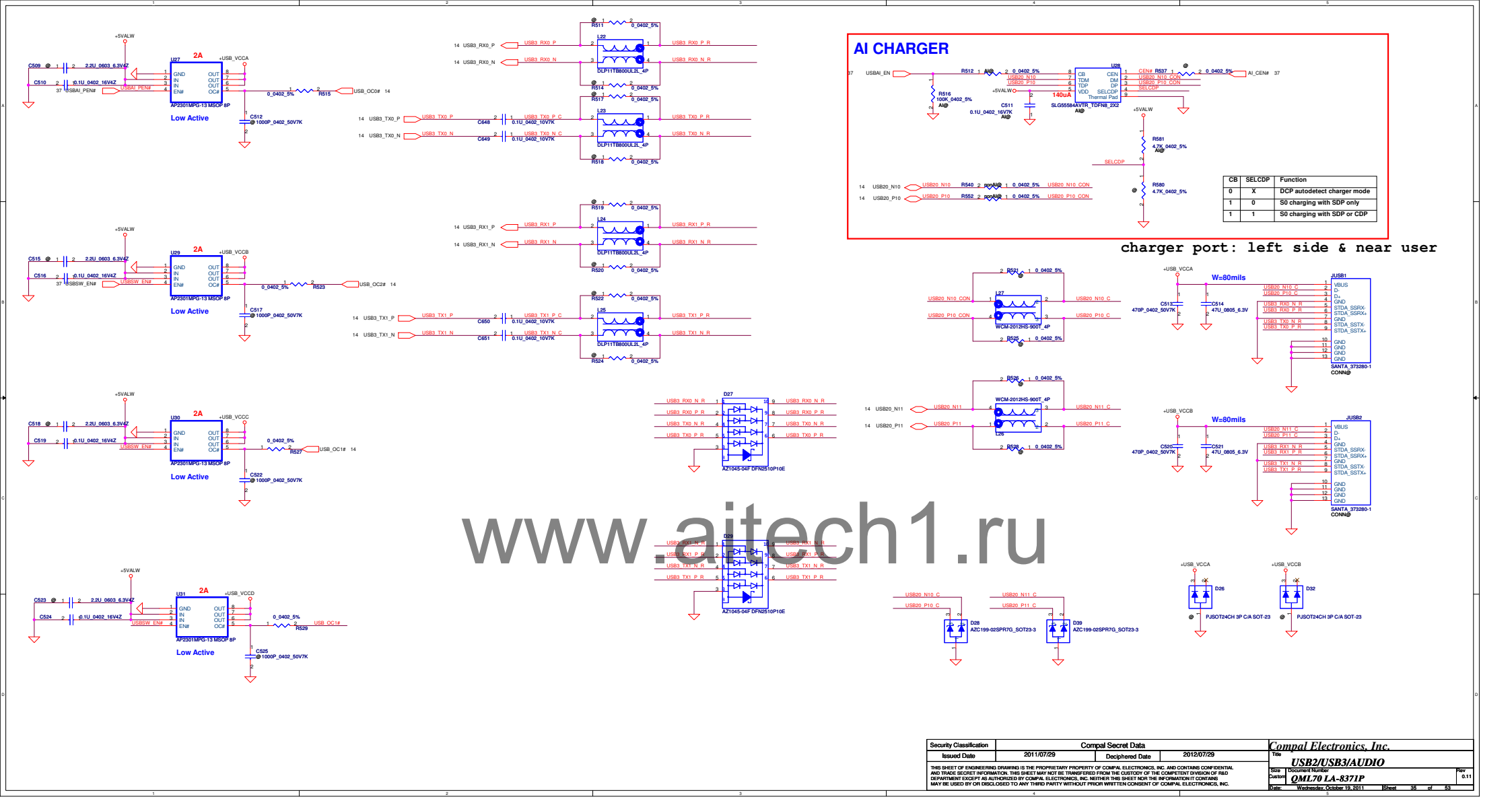
Compal Electronics, Inc.

Title: P28-HDD & ODD CONN

Size: B | Document Number: QML70 LA-8371P | Rev: 0.11

Date: Wednesday, October 19, 2011 | Sheet 34 of 53



CB	SELCDP	Function
0	X	DCP autodetect charger mode
1	0	S0 charging with SDP only
1	1	S0 charging with SDP or CDP

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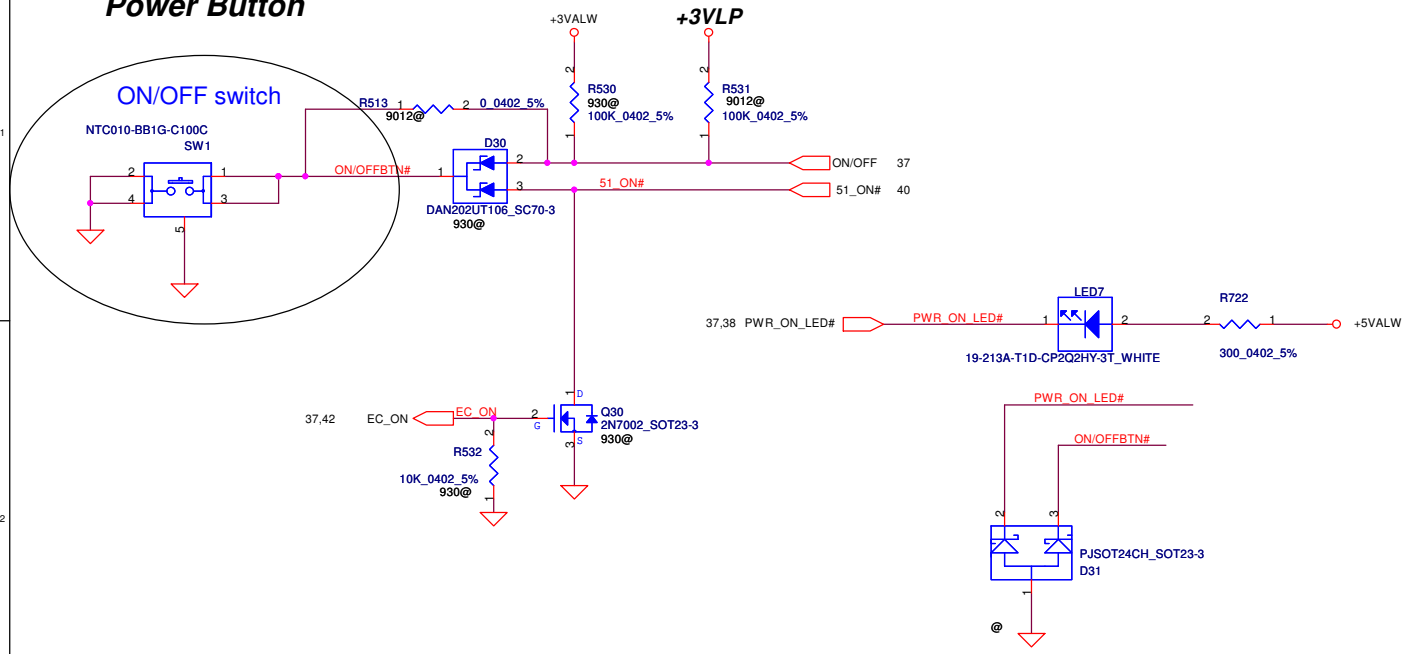
Compal Electronics, Inc.

Title: USB2/USB3/AUDIO

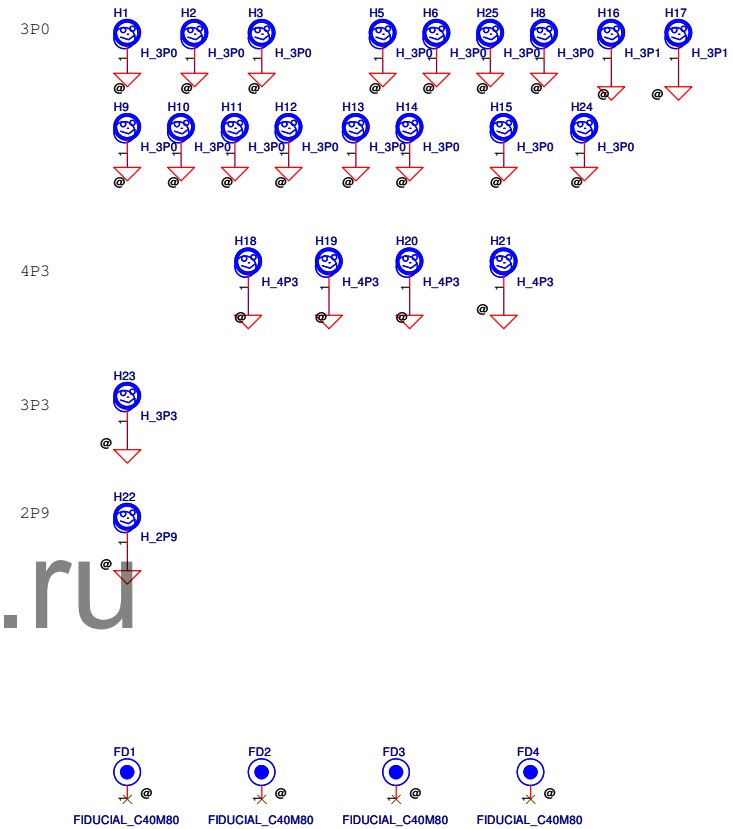
Size: Custom | Document Number: QML70 LA-8371P | Rev: 0.11

Date: Wednesday, October 19, 2011 | Sheet 35 of 53

Power Button



Screw Hole



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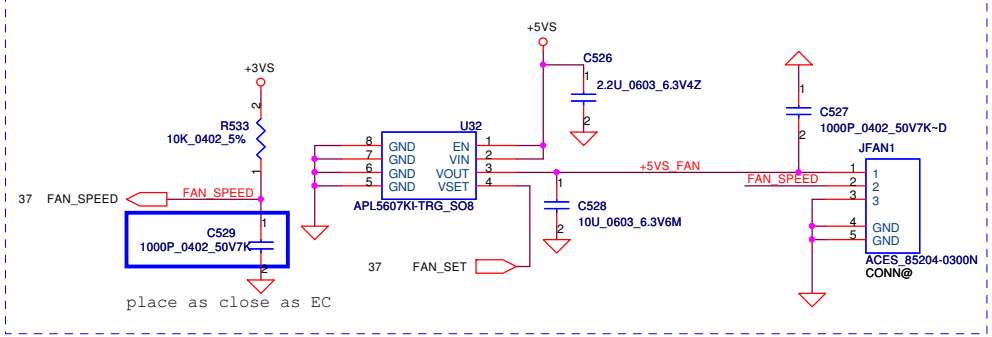
Fan Control Circuit



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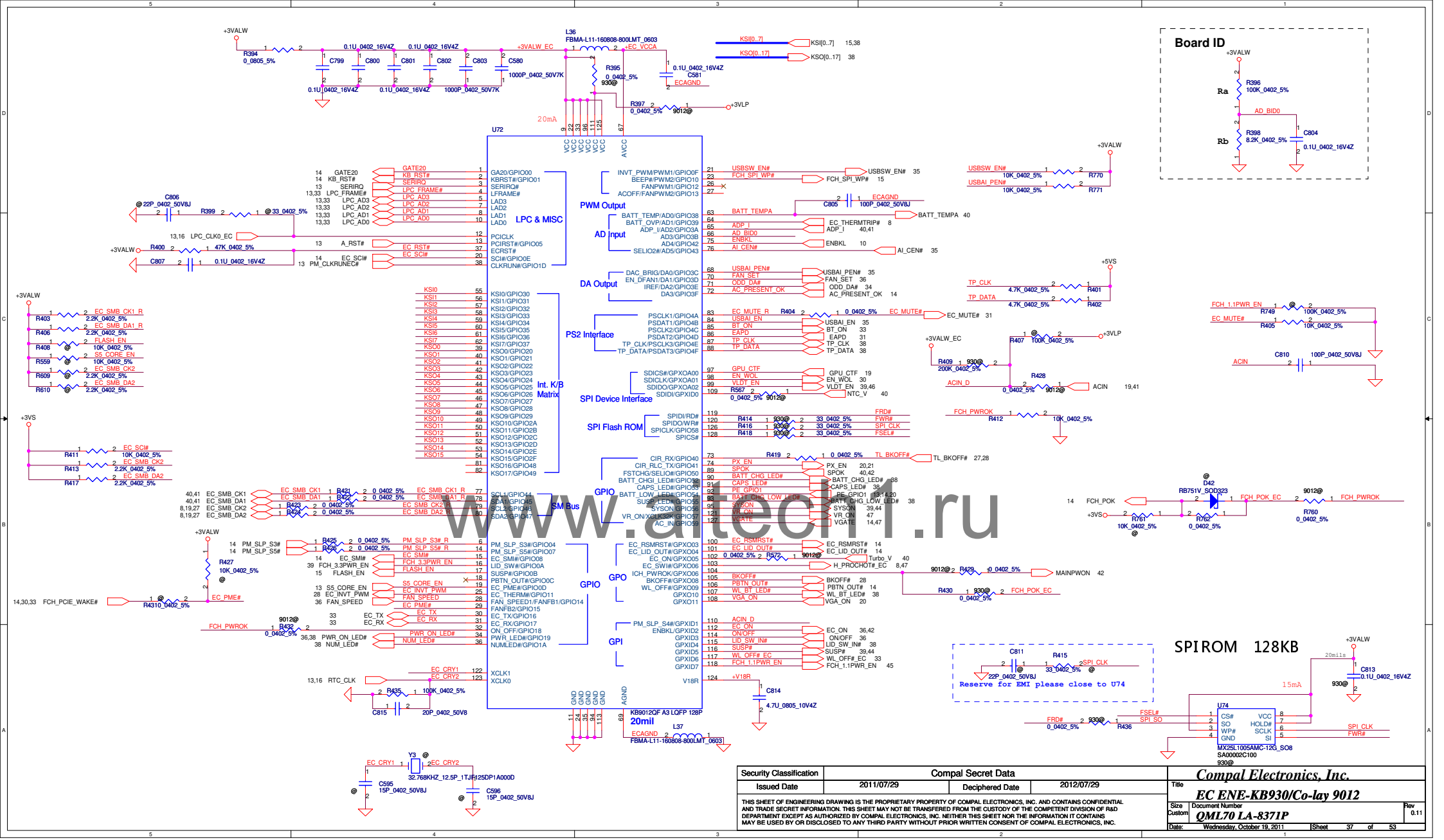
Compal Electronics, Inc.

Title: PWRBTN/ FAN / Screws

Size: Custom | Document Number: QML70 LA-8371P | Rev: 0.11

Date: Wednesday, October 19, 2011 | Sheet 36 of 53



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Issued Date	2011/07/29	Deciphered Date	2012/07/29

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Compal Electronics, Inc.

Title: EC ENE-KB930/Co-lay 9012

Size: Custom | Document Number: QML70 LA-8371P | Rev: 0.11

Date: Wednesday, October 19, 2011 | Sheet 37 of 53

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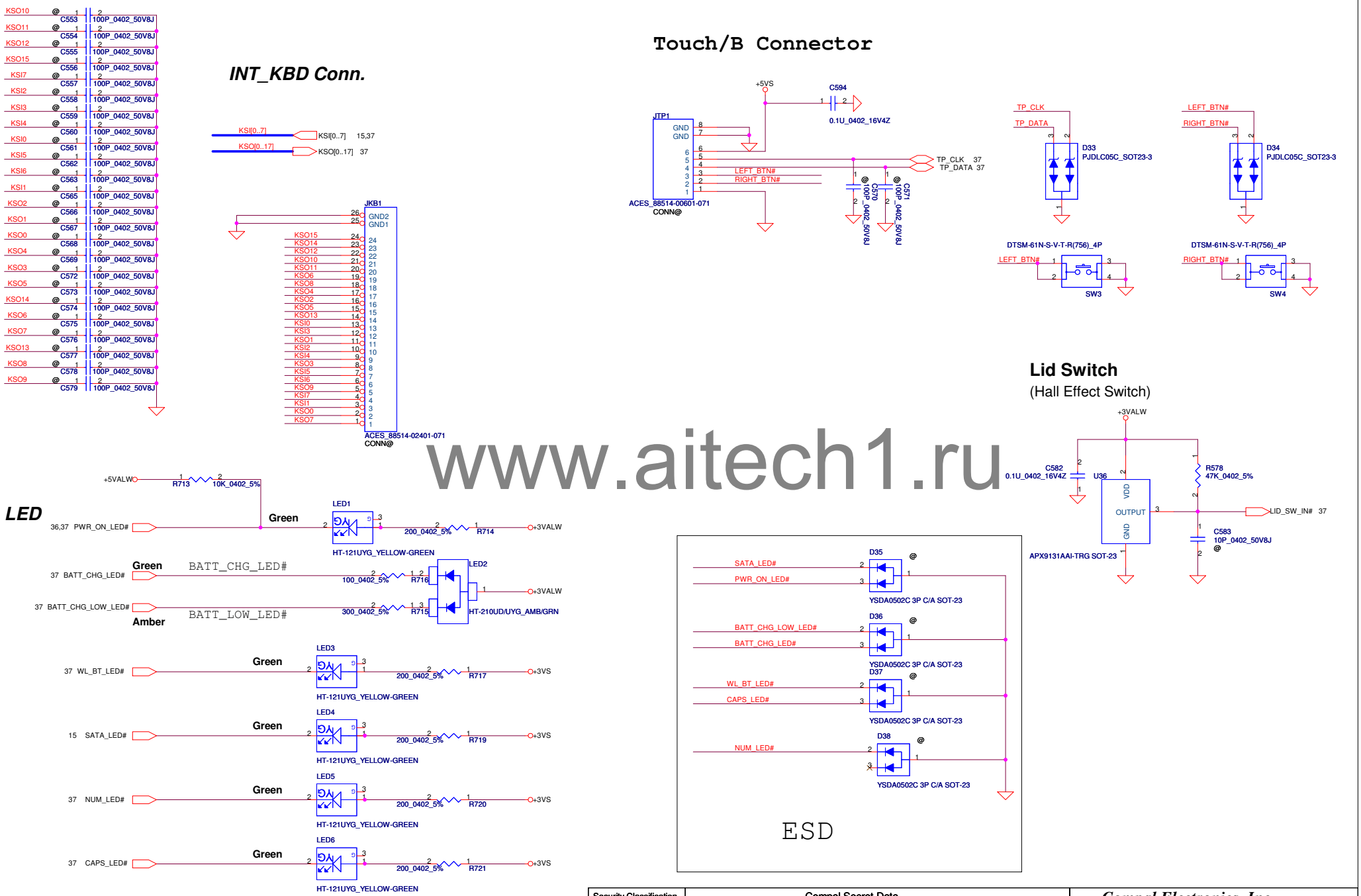

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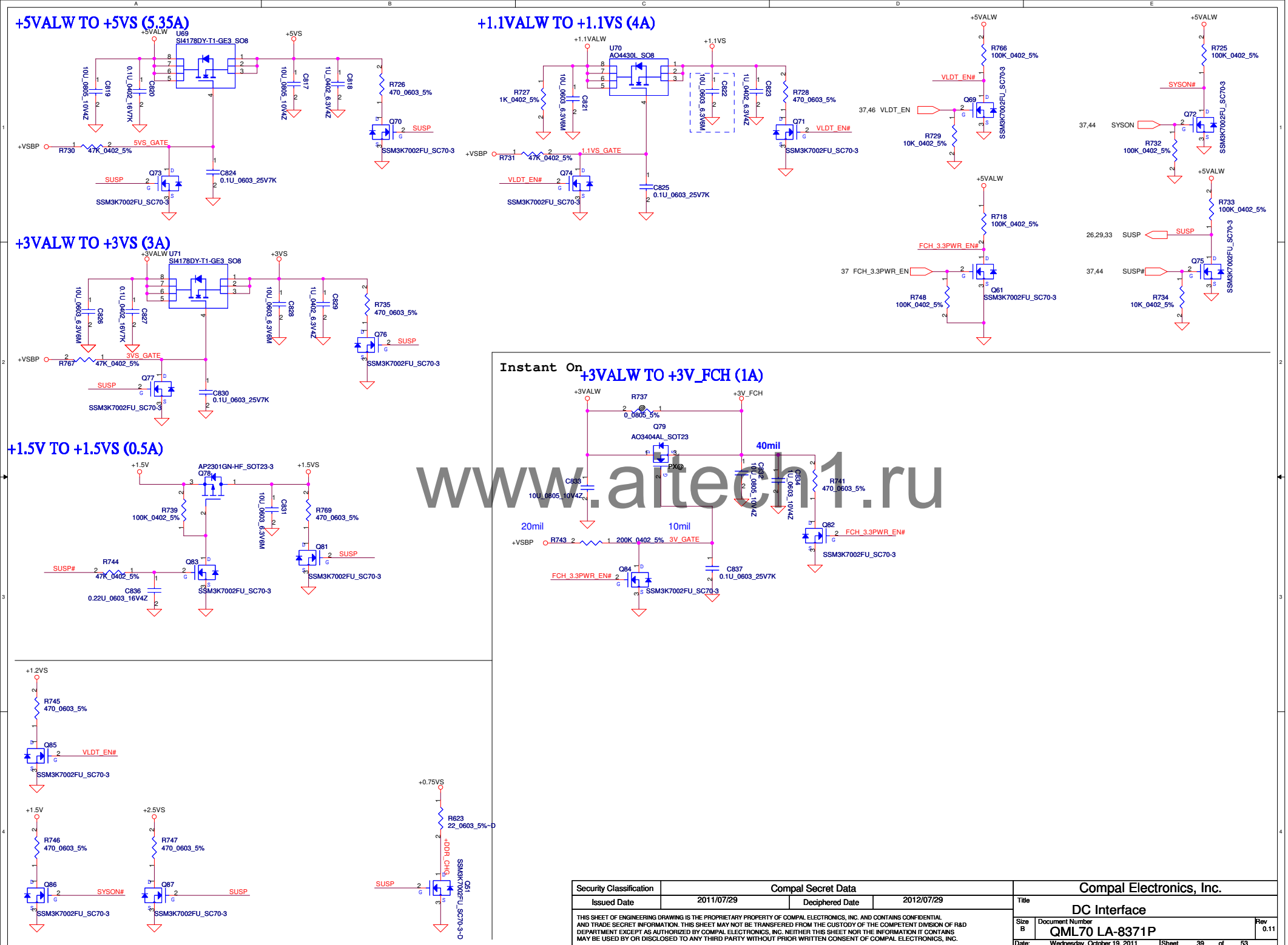
Compal Electronics, Inc.

Title: KB/EC ROM/TP/FUN/LED

Size: B | Document Number: QML70 LA-8371P | Rev: 0.2

Date: Wednesday, October 19, 2011 | Sheet 38 of 53



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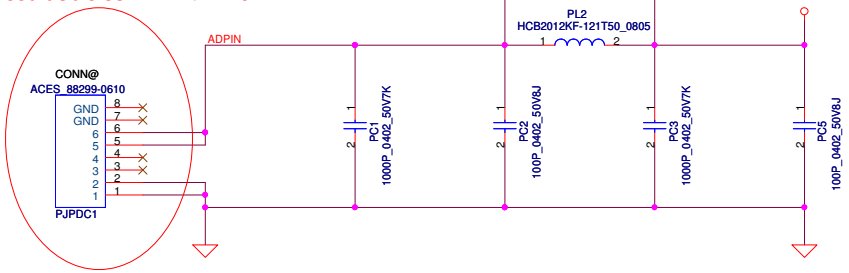
Compal Electronics, Inc.

Title: DC Interface

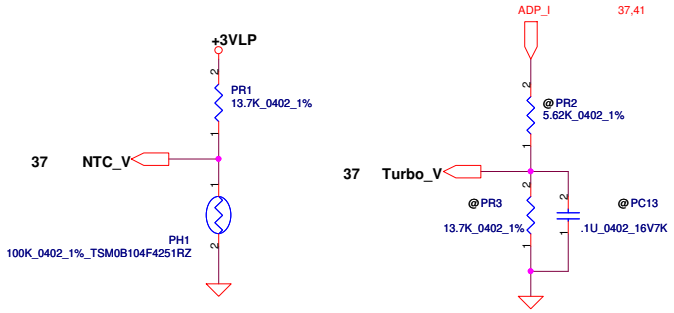
Size: B | Document Number: QML70 LA-8371P | Rev: 0.11

Date: Wednesday, October 19, 2011 | Sheet 39 of 53

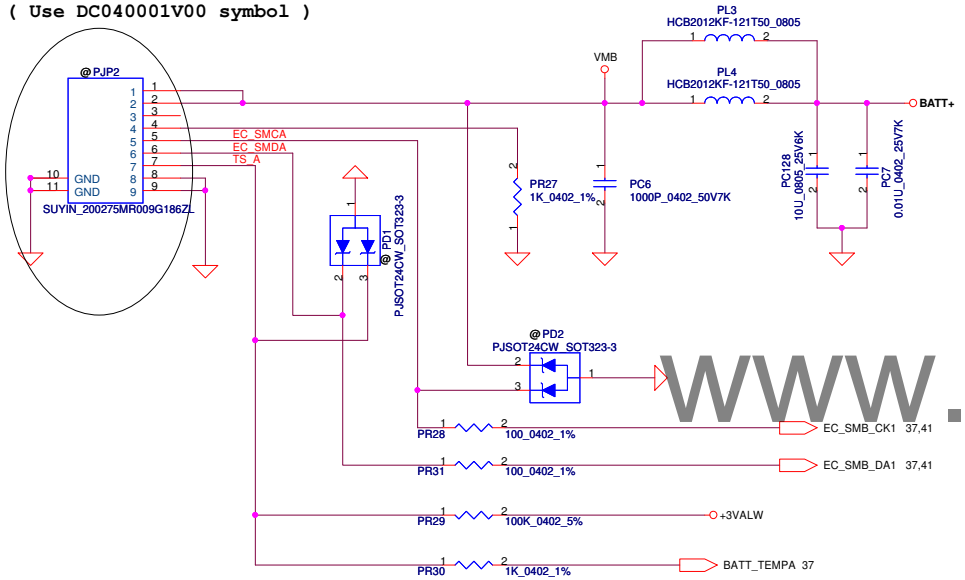
DCIN jack P/N:SP02000N000,
need doble confirm P/N with ME

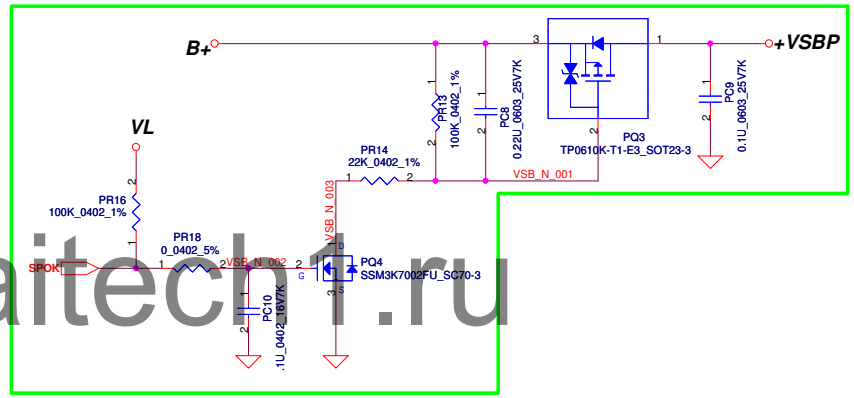


PH901 under CPU botten side :
CPU thermal protection at 90 degree C
Recovery at 50 degree C



Change DC040007T0L to DC040004L00
(Use DC040001V00 symbol)





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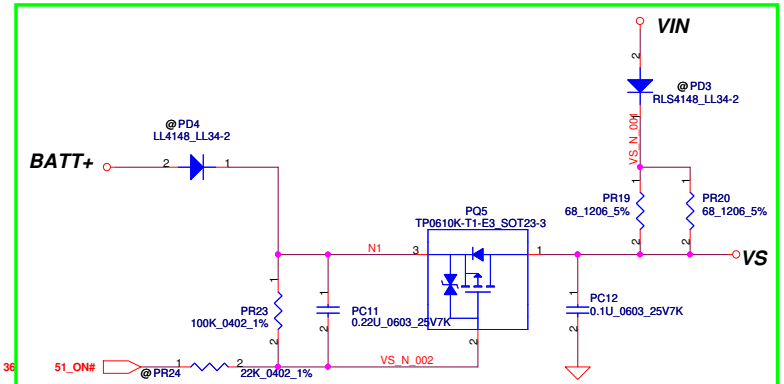
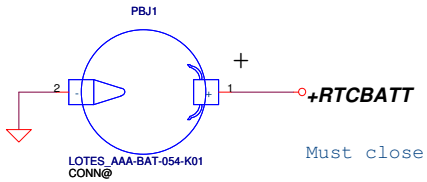


For KB9012 --> Remove all 51_ON# circuit

RTC Battery



Must close PBJ1

Change RTC For Cost Down
SP07000H700

Security Classification	Compal Secret Data		
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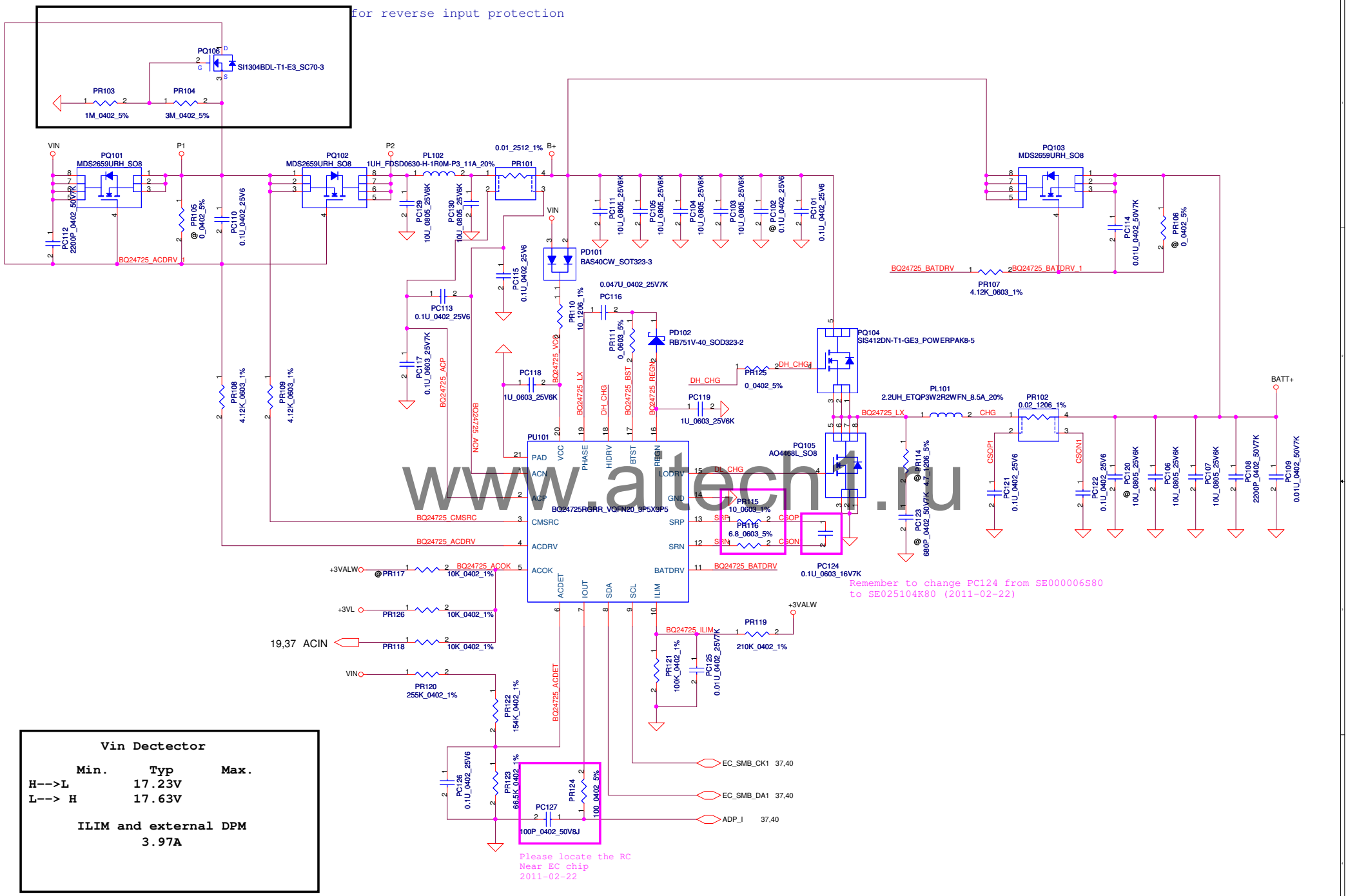
Compal Electronics, Inc.

Title: PWR-DCIN / BATT CONN / OTP

Size: | Document Number: QML70 LA-8371P | Rev: 0.2

Date: Wednesday, October 19, 2011 | Sheet 40 of 53



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Vin Dectector

	Min.	Typ	Max.
H-->L		17.23V	
L--> H		17.63V	

ILIM and external DPM
3.97A

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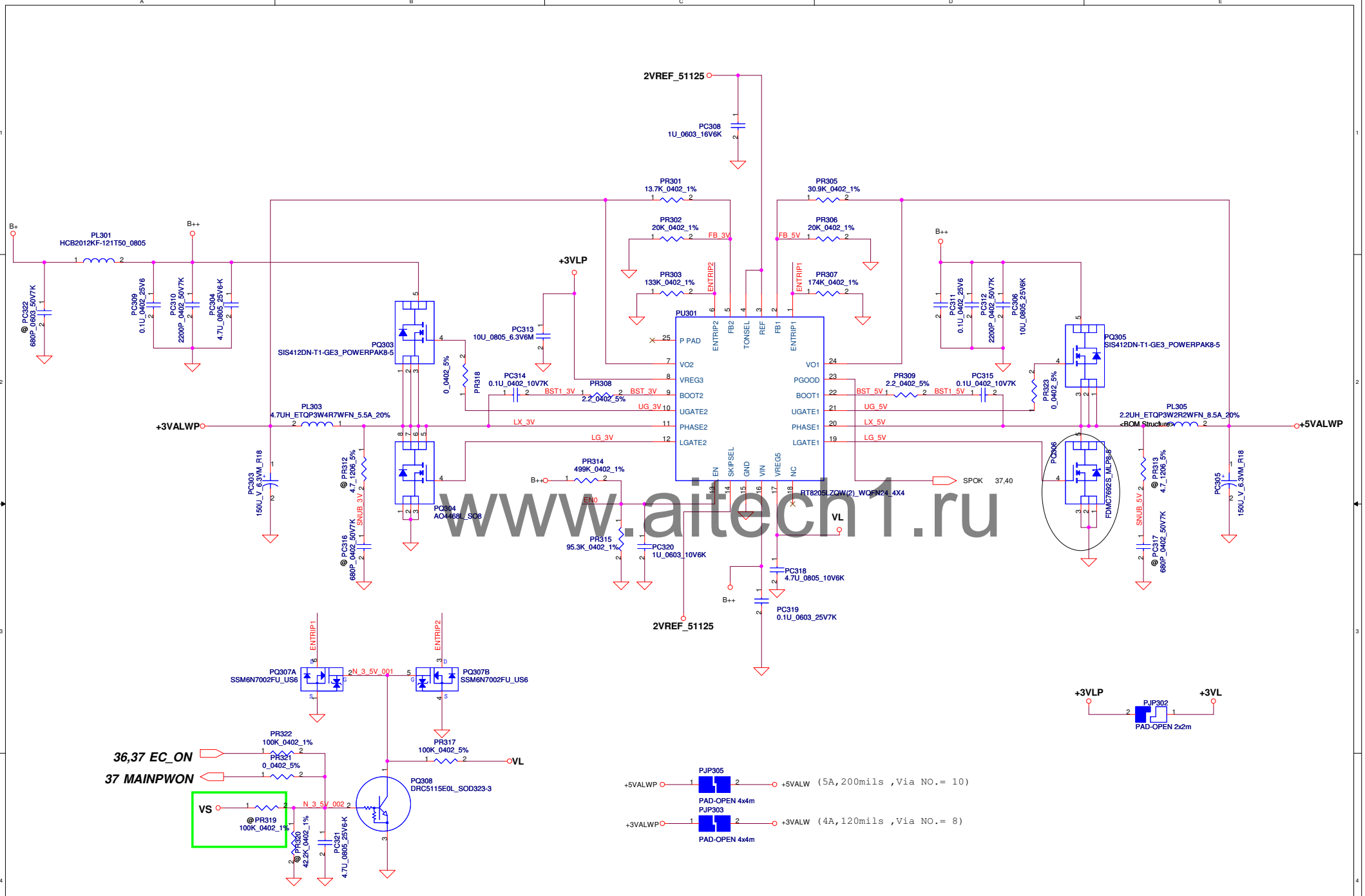
Compal Electronics, Inc.

Title: **PWR-CHARGER**

Size | Document Number: *QML70 LA-8371P* | Rev: 0.2

Date: Wednesday, October 19, 2011 | Sheet 41 of 53



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For KB930 --> Keep PR319, Remove PR322
For KB9012 (Red square) --> Remove PR319
Keep PR322

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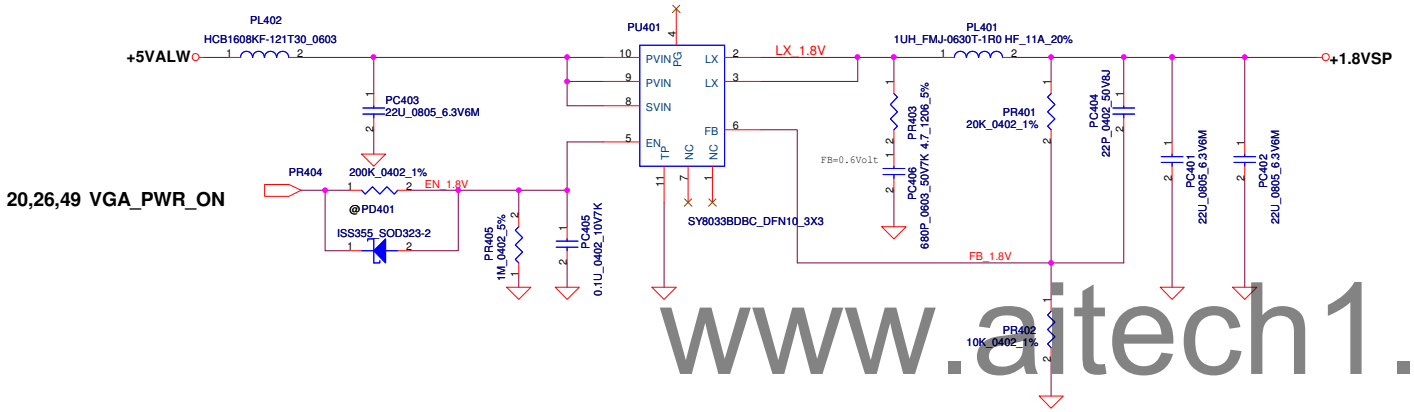
Compal Electronics, Inc.

Title: **PWR-3.3VALWP/5VALWP**

Size: Custom | Document Number: QML70 LA-8371P | Rev: 0.01

Date: Wednesday, October 19, 2011 | Sheet 42 of 51



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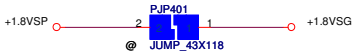

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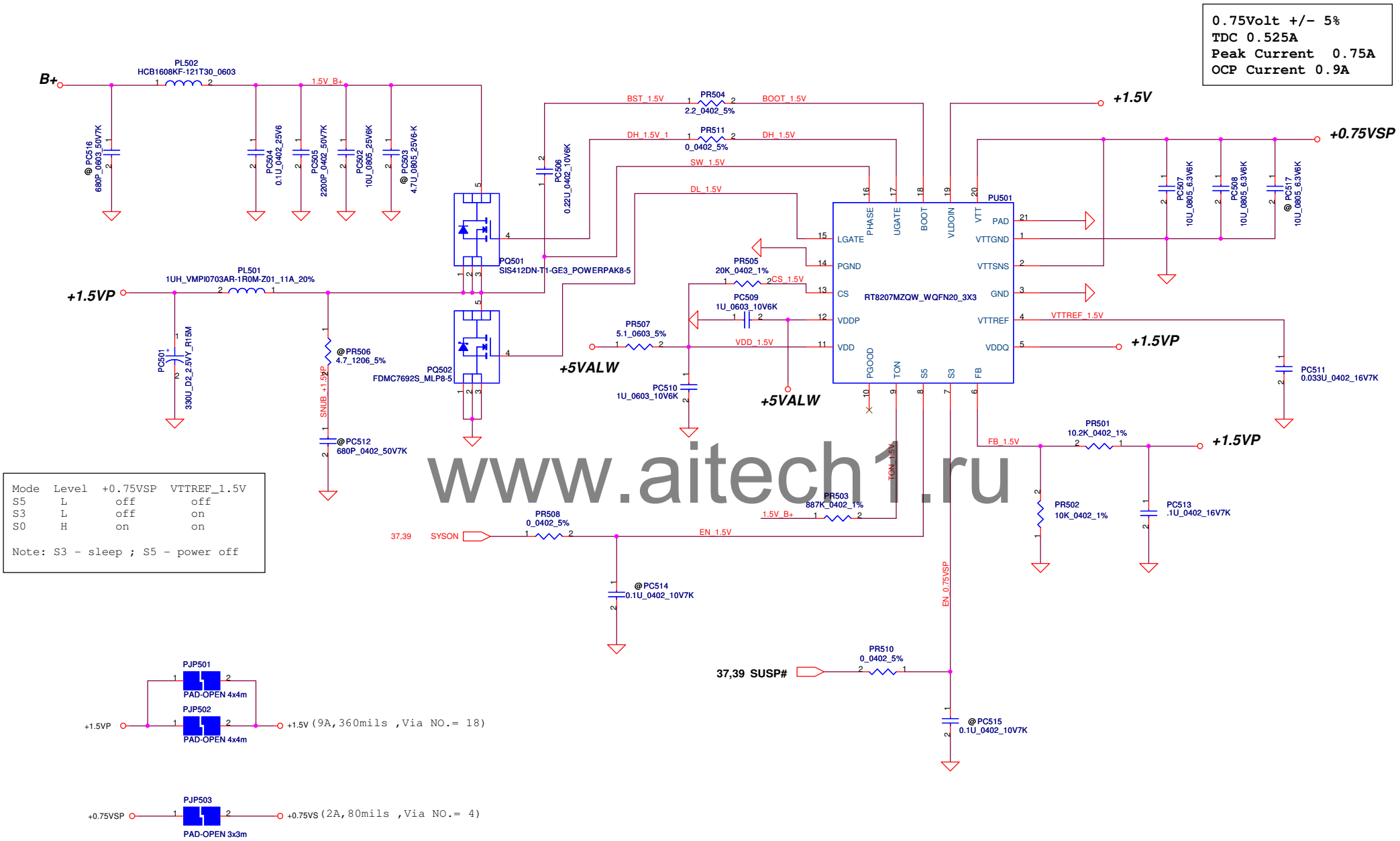
Compal Electronics, Inc.

Title: **+1.8VP**

Size | Document Number: QML70 LA-8371P | Rev: 0.01

Date: Wednesday, October 19, 2011 | Sheet 43 of 51



Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

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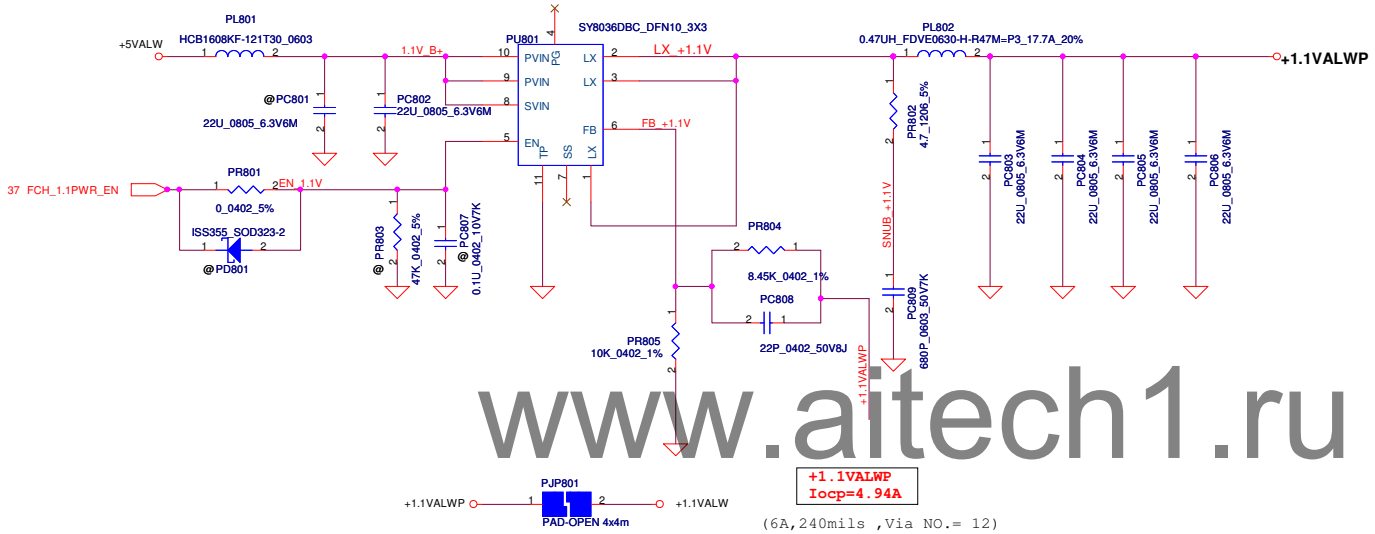
Compal Electronics, Inc.

Title: **PWR-1.5VP / +0.75VSP**

Size: Custom | Document Number: QML70 LA-8371P | Rev: 0.01

Date: Wednesday, October 19, 2011 | Sheet 44 of 51



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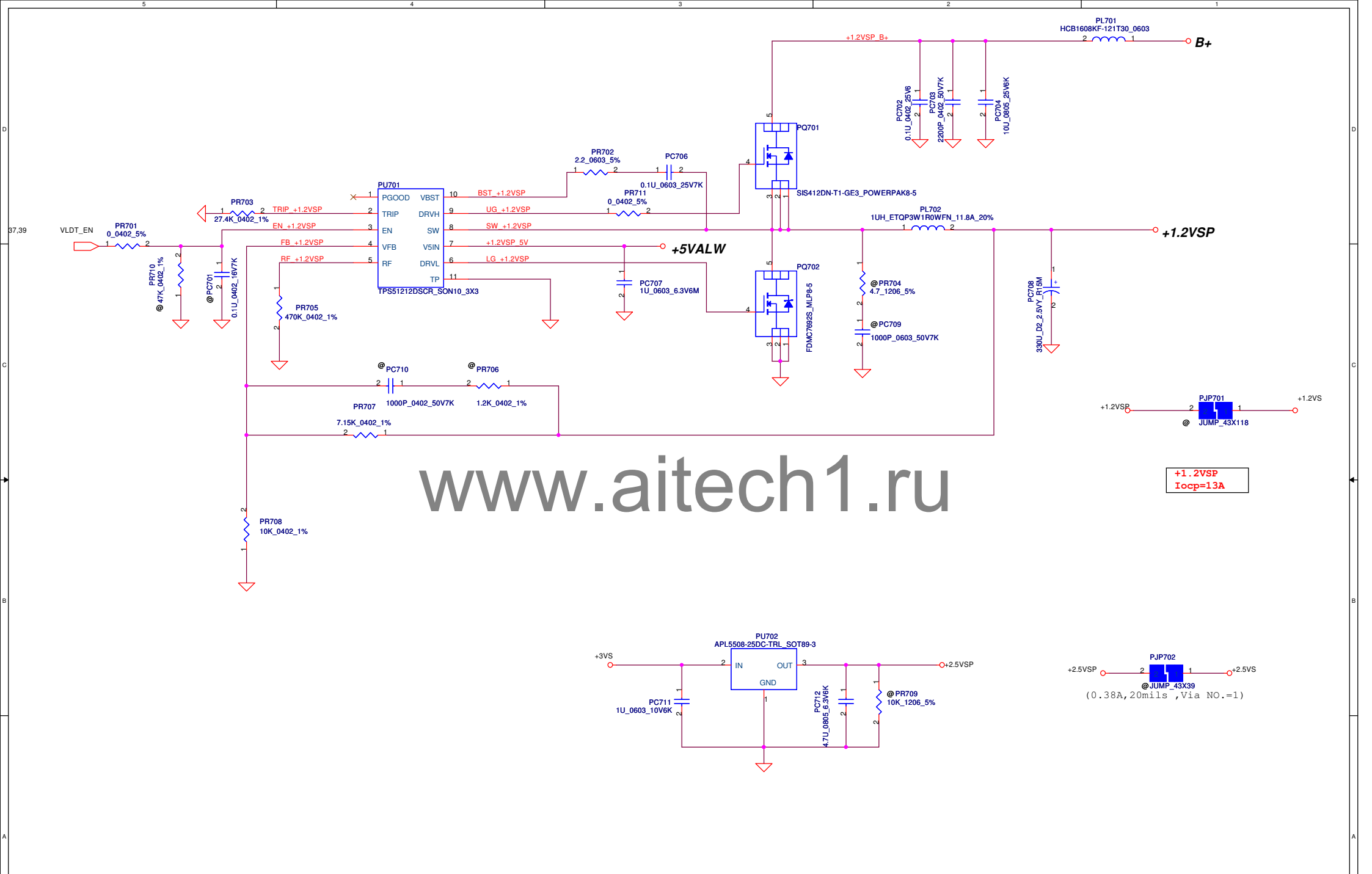
Compal Electronics, Inc.

Title: **+1.1VALWP**

Size	Document Number	Rev
	QML70 LA-8371P	0.01

Date: Wednesday, October 19, 2011 | Sheet 45 of 51



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Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/07/29	Deciphered Date	Title: +1.2VSP/+2.5VSP
			Size: Document Number: QML70 LA-8371P Rev: 0.01
			Date: Wednesday, October 19, 2011 Sheet 46 of 51

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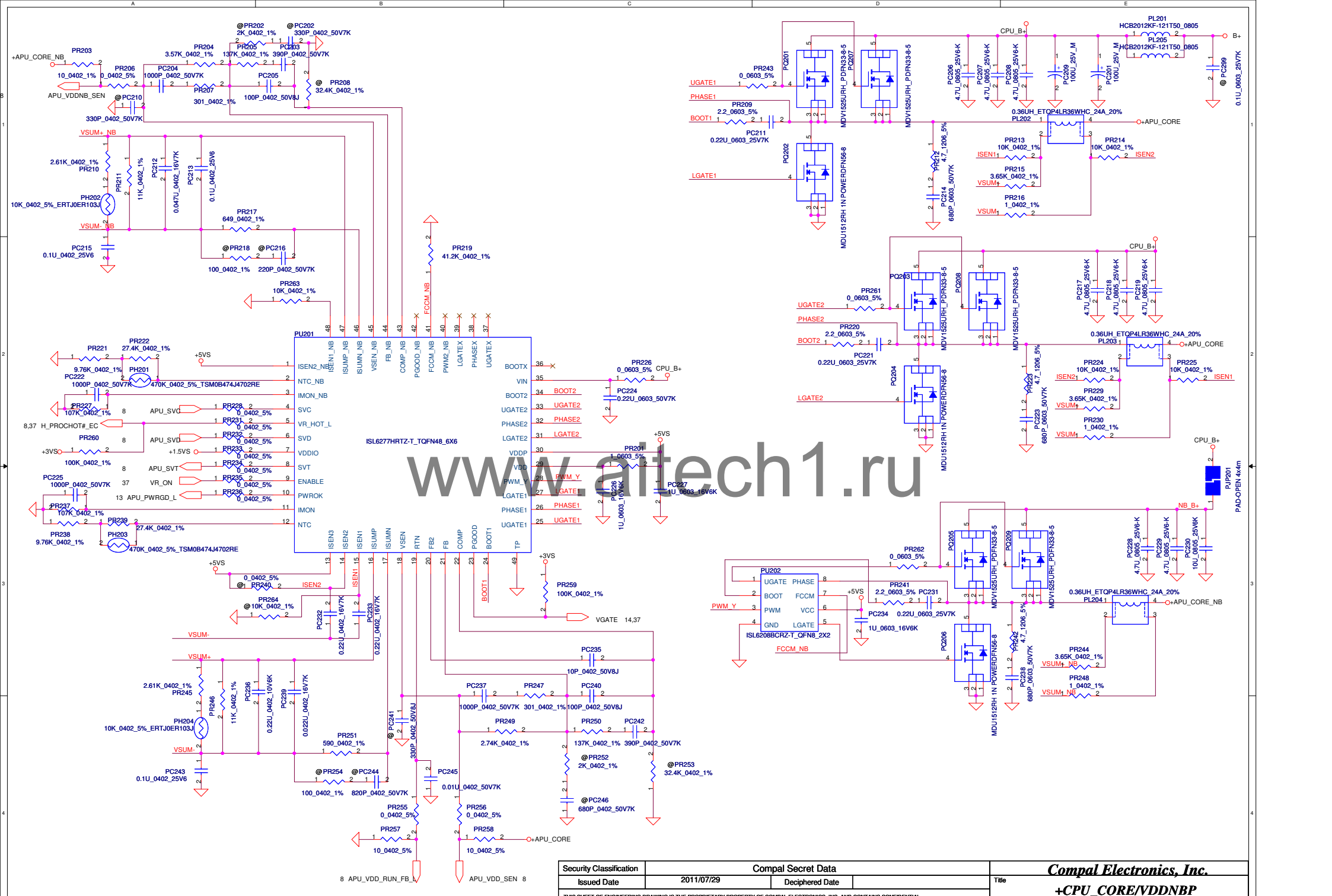

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Compal Electronics, Inc.

Title: **+CPU_CORE/VDDNBP**

Size	Document Number	Rev
Custom	QML70 LA-8371P	0.01

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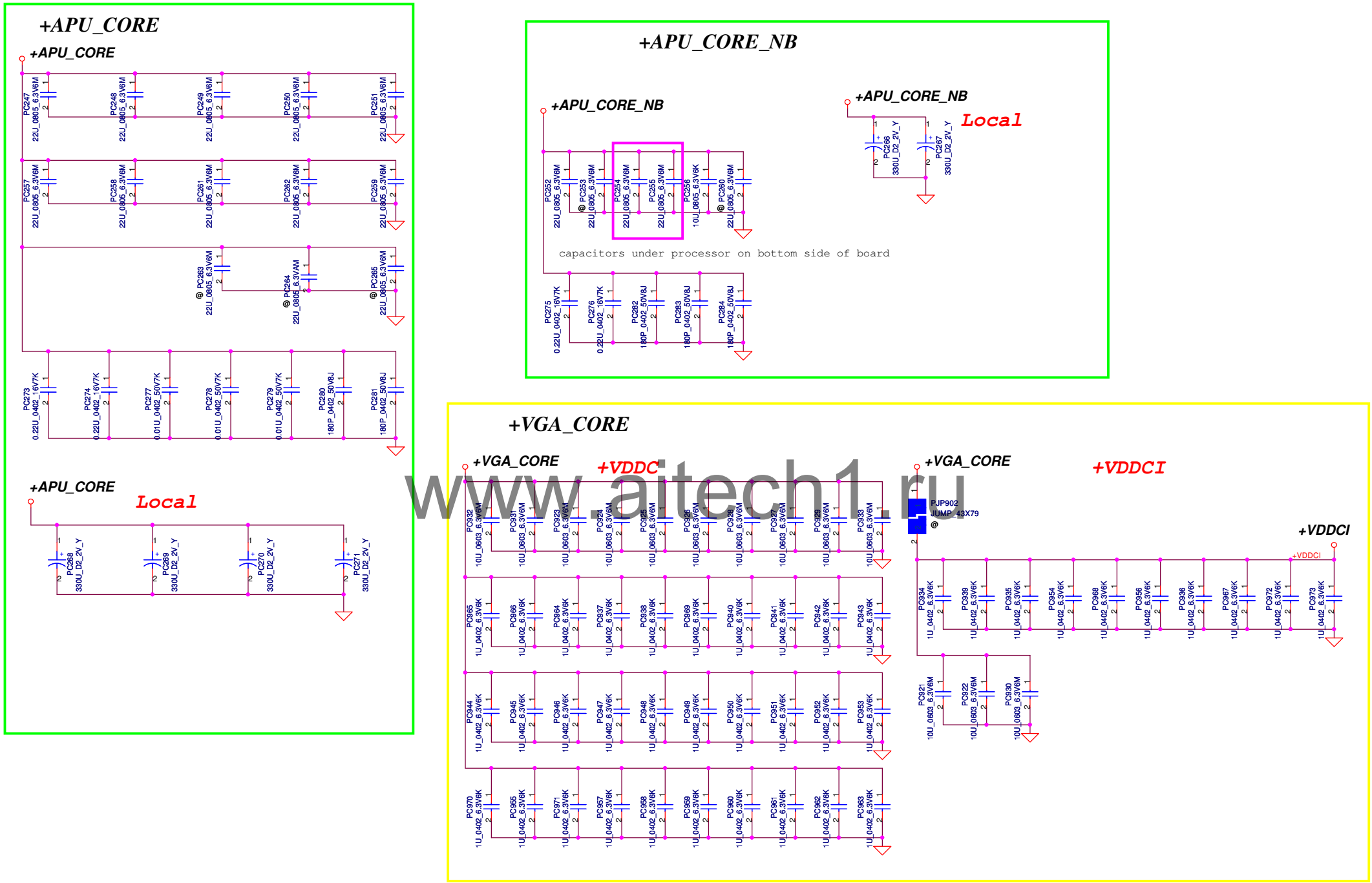

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Compal Electronics, Inc.

Title: **PROCESSOR DECOUPLING**

Size	Document Number	Rev
A3	QML70 LA-8371P	0.01

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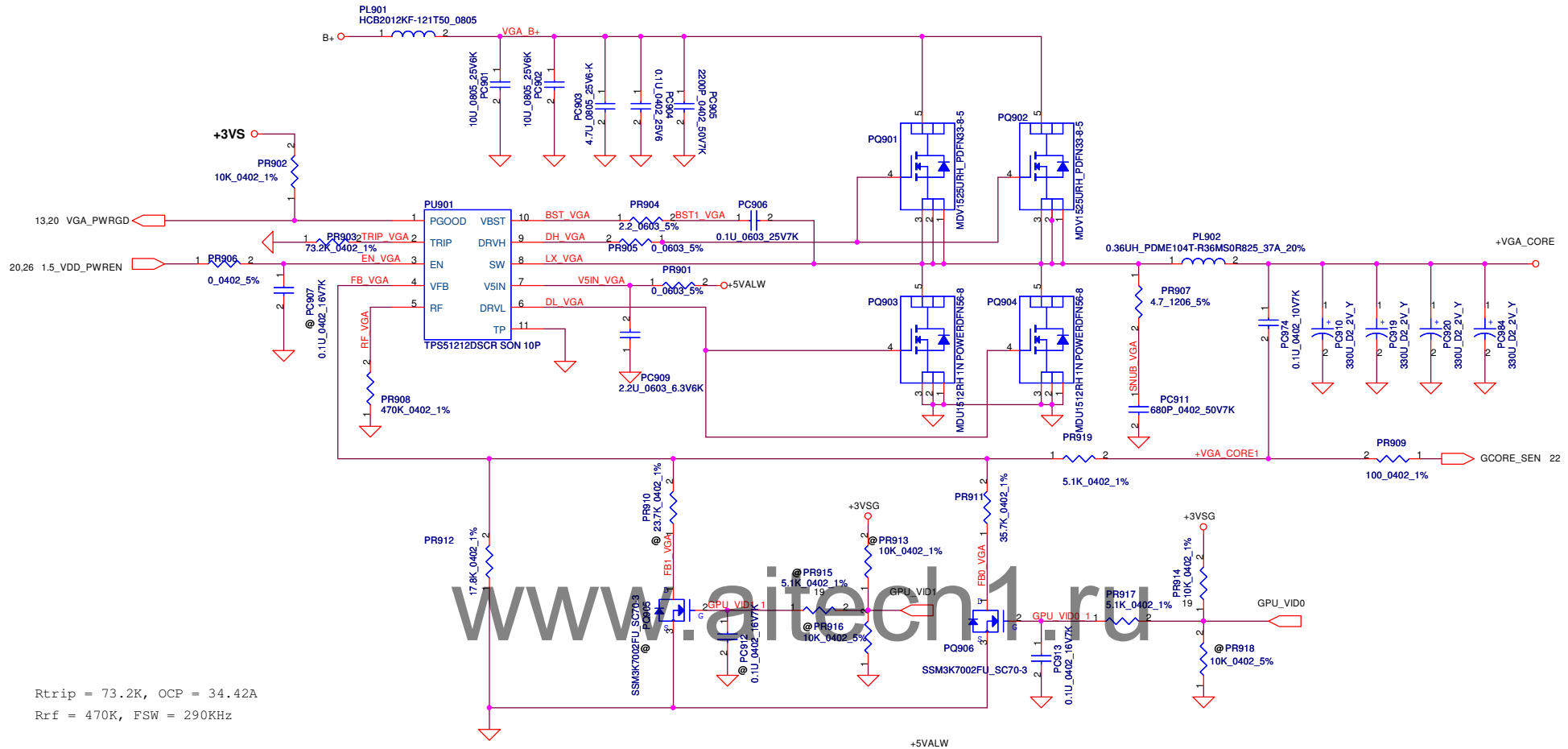

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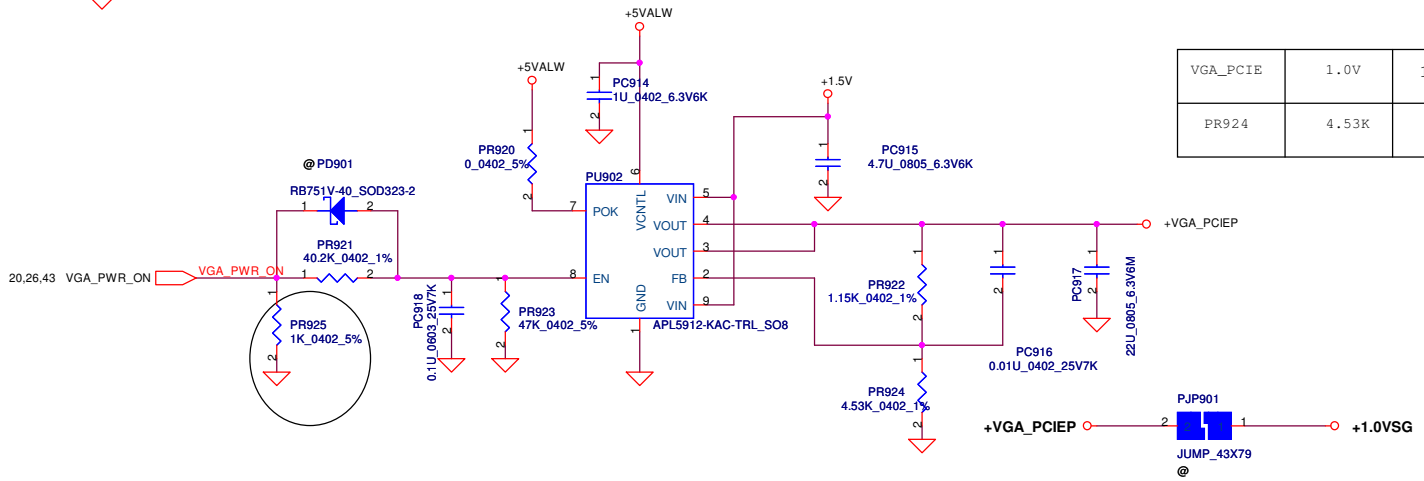
Rtrip = 73.2K, OCP = 34.42A

Rrf = 470K, FSW = 290KHz



VGA_PCIE	1.0V	1.1 V
PR924	4.53K	3K

For Whistler (Thames)
1/2Delta I=4.05A
Vtrip=36.5K*10uA=0.365V
Iocpmin=0.365V/(8*1.6m)+1/2Delta I=28.51A+4.05A
=32.56A

	Thames
GPU_VID0	Core Voltage Level
1	0.9V
0	1.0V

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Compal Electronics, Inc.

Title: **VGA_CORE**

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Version Change List (P. I. R. List) for Power Circuit

Page#	Title	Date	Request Owner	Issue Description	Solution Description

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Base on GPU Reference schematic	0.02	22	Reserve pull-up / pull-down resistor 100ohm on GCORE_SEN	08/30	SR
2			0.02	15	Modify Netname of SPI signal of U5	08/30	SR
3			0.02	26	Change Q91.2 from 1.5_VDDC_PWREN# to 1.5VSG_PWREN#	08/30	SR
4		These components are for VGA	0.02	26	Change BOM Structure of R349, R350, R354, R355, Q95, Q96 to PX@	08/30	SR
5		Base on AMD Comal CRB	0.02	8	Change pull-up voltage of APU_RST#, APU_PWRGD, APU_SVT, APU_SVC, APU_SVD, ALERT_L, ALLOW_STOP from +1.5V to +1.5VS	08/30	SR
6		For EMI request	0.02	15	Reserve R559, R561, C624, C625 @ FCH_SDCLK / FCH_SDWP	08/30	SR
7			0.02	36	Remove USB3.0 Host contorller circuit	09/01	SR
8			0.02	17	Remove componets of HUDSON_M2	09/01	SR
9		Set PCIE FULL TX OUTPUT SWING to High (Full Swing)	0.02	19	Modify GPU Straps: GPU_GPIO0 pull-high	09/01	SR
10			0.02	23	Reserve pull-high and pull-down resistor of MAA14/MBB14	09/01	SR
11		Base on Thames M2 datasheet	0.02	21	Modify U7.U13, U7.14 to NC	09/01	SR
12			0.02	19	Add THM_ALERT# to from U7.AG30 (GPU_THERMAL INT) to U34.6 (ADM1032) Add GPU_CTF from U7.AM17 (GPU_CTF) to U72.97 (EC)	09/02	SR
13			0.02	31	Reserve Analog mircophone circuit	09/02	SR
14			0.02	9, 39,45	Change contorl singal of 1.1VALWP from SP0K to FCH_1.1PWR_EN Change +1.1V_FCH to +1.1VALW	09/02	SR
15			0.02	15,37	Connect U72.92 (EC) to U2.V1 (FCH)for SYS ROM Write Protect	09/02	SR
16			0.02	35	Co-lay AI Charger	09/02	SR
17			0.03	31	Modify Analog Microhpone circut base on Vendor suggestion	09/05	SR
18			0.03	22	Add decoupling cap. base on GPU check list	09/06	SR
19			0.03	17	Change decoupling cap. base on FCH check list	09/06	SR
20			0.03	27	Change LVDS translator to RTD2136	09/06	SR
21			0.03	28	Add pull-up resistor R129, R132 (2.2K) of FCH_CRT_DDC_SDA / SCL	09/06	SR
22			0.03	13	Change R99 to 22ohm (CLK_SD_48M)	09/07	SR
23			0.03	14	Pull-down PEG_CLKREQ#	09/08	SR
24			0.03	37	Change Board ID, R398: 0ohm	09/08	SR
25			0.03	34	Change Power source of ODD from +5VS to +5VALW	09/09	SR
26			0.03	33	Change Power source of WLAN from +3VALW to +3VS	09/09	SR
27			0.03	32	Add power source for none Card Reader IC solution	09/09	SR

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Title: HW-PIR1

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1			0.2	15	Change U5 power from +3V_PCH to +3V_FCH	10/11	SR2
2			0.2	15	Change GBE_MDIO pull-up voltage from +3VALW to +3V_FCH	10/11	SR2
3	Blue Screen after install VGA Driver		0.2	25	SWAP QSB7 and QSB#7	10/11	SR2
4			0.2	32	Delete Net SDCD, SDWP# that connect to EC Add MOSFET inverter of SDWP#	10/11	SR2
5			0.2	8	Un-mount pull-high resistor of APU_SVT, APU_SVC, APU_SVD	10/11	SR2
6			0.2	28	Follow QCL70 pin define	10/11	SR2
7			0.2	38	Modify Touch Pad pin define	10/11	SR2
8		For voltage leakage	0.2	8	Change pull-high voltage of APU_PROCHOT#, APU_THERMTRIP#, APU_SVT, APU_SVC, APU_SVD, ALERT_L, ALLOW_STOP, APU_RST#, APU_PWRGD, APU_SIC, APU_SID	10/11	SR2
9		Base on AMD recommend	0.2	24, 25	Change R299, R300, R309, R310, R319, R320, R325, R326 from 56ohm to 40.2ohm	10/11	SR2
10			0.2	37	Change Board ID to "1" for SR2	10/13	SR2
11			0.2	22	Seperate VDDC and VDDCI of VGA	10/14	SR2
12			0.2	23	Reserve R611, R612 for MAA14, MAB14	10/14	SR2
13							
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15							
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Compal Electronics, Inc.

Title: HW-PIR2

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